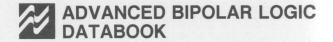
ADVANCED
BIPOLAR LOGIC
DATABOOK

NATIONAL SEMICONDUCTOR CORPORATION





#### Introduction

This is the Advanced Bipolar Logic Databook from National Semiconductor. The book contains the most up to date information on the Advanced Schottky and Advanced Low Power Schottky families available from National.

Both of these advanced logic families are in their early production phases and will be continually expanded in future National Databook Publications.

Contact your National Semiconductor Representative for more information concerning these next generation logic families or any of the other extensive logic families.

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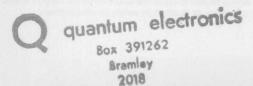
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#### LIFE SUPPORT POLICY

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- A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



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### A+ Program

**A+ Program:** A comprehensive program that utilizes National's experience gained from participation in the many Military/Aerospace programs.

A program that not only assures high quality but also increases the reliability of molded integrated circuits.

The A+ program is intended for users who cannot perform incoming inspection of ICs or do not wish to do so, yet need significantly better than usual incoming quality and higher reliability levels for their standard integrated circuits.

Users who specify A+ processed parts will find that the program:

- · Eliminates incoming electrical inspection.
- Eliminates the need for, and thus the added cost of, independent testing laboratories.
- · Reduces the cost of reworking assembed boards.
- · Reduces field failures.
- · Reduces equipment down time.
- Reduces the need for excess inventories due to yield loss incurred as a result of processing performed at independent testing laboratories.

#### The A+ Program Saves You Money

It is a widely accepted fact that down-time of equipment is costly not only in lost hours of machine usage but also costly in the reapir and maintenance cycle. One of the added advantages of the A+ program is the burn-in screen, which is one of the most effective screening procedures in the semiconductor industry. Failure rates as a result of the burn-in can be decreased many times. The objective of burn-in is to stress the device much higher that it would be stressed during normal usage.

#### Reliability vs. Quality

The words "reliability" and "quality" are often used interchangeably, as though they connoted identical facets of a product's merit. But reliability and quality are different, and IC users must understand the essential difference between the two concepts in order to evaluate properly the various vendors' programs for products improvement that are generally available, and National's A+ program in particular.

The concept of quality gives us information about the population and faulty IC devices among good devices, and generally relates to the number of faulty devices that arrive at a user's plant. But looked at in another way, quality can instead relate to the number of faulty ICs that escape detection at the IC vendor's plant.

It is the function of a vendor's Quality Control arm to monitor the degree of success of that vendor in reducing the number of faulty ICs that escape detection. Quality Control does this by testing the outgoing parts on a sampled basis. The Acceptable Quality Level (AQL) in turn determines the stringency of the sampling. As the AQL decreases it becomes more difficult for defective parts to escape detection, thus the quality of the shipped parts increases.

The concept of reliability, on the other hand, refers to how well a part that is initially good will withstand its environment. Reliability is measured by the percentage of parts that fail in a given period of time.

Thus the difference between quality and reliability means the ICs of high quality may, in fact be of low reliability, while those of low quality may be of high reliability.

#### Improving the Reliability of Shipped Parts

The most important factor that affects a part's reliability is its construction: the materials used and the method by which they are assembled.

Reliabilty cannot be tested into a part. Still, there are tests and procedures that an IC vendor can implement which will subject the IC to stresses in excess of those that it will endure in actual use, and which will eliminate marginal, short-life parts.

In any test of reliability the weaker parts will normally fail first. Further, stress tests will accelerate, or shorten, the time of failure of the weak parts. Because the stress tests cause weak parts to fail prior to shipment to the user, the population of shipped parts will in fact demonstrate a higher reliability in use.

#### National's A+ Program

National has combined the successful B+ program with the Military/Aerospace processing specifications and provides the A+ program as the best practical approach to maximum quality and reliability on molded devices. The following flow chart shows how we do it step by step.

Randomly selected wafers are taken from production regularly and subjected to SEM analysis. **Epoxy B Processing for All Molded Parts** At National, all molded semiconductors, including ICs, have been built by this process for some time now. All processing steps, inspections, and QC monitoring are designed to provide highly reliable products. (A reliability report is available that gives, in detail, the background of Epoxy B, the reason for its selection at National, and reliability data that proves its success.) Six Hour, 150°C Bake This stress places the die bond and all wire bonds into a combined tensile and shear stress mode, and helps eliminate marginal bonds and electrical connections.

+	High Temperature (100°C) Functional Electrical Test A high temperature test with voltages applied places the die under the most severe stress possible. The test is actually performed at 100°C-30°C higher than the commercial ambient limit. All devices are thoroughly exercised at the 100°C ambient.
中	Electrical Testing Every device is tested at 25°C for functional and DC parameters.
Ť	Burn-in Test Devices are stressed at maximum operating conditions to eliminate marginal devices. Test is performed per Mil-Std-883B Method 1015.3.
中	DC Functional and Parametric Tests These room-temperature functional and parametric tests are the normal, final tests through which all National products pass.
-	Thermal Shock Monitor  Samples from each package type are selected at random each week and submitted to 100 cycles of liquid to liquid thermal shock -65°C to +150°C. In addition, samples are selected every four weeks and subjected to 2000 temperature cycles of 0°C to +25°C.
Ť	Tighter-than-normal QC Inspection Plans Most vendors sample inspect outgoing parts to a 0.3% AQL. When you specify the A+ program, we sample your parts to a 0.035% AQL at room temperature and 0.05% AQL at T <sub>A</sub> Max. This eight times tightening (from 0.3 to 0.035% AQL) coupled with three 100% electrical tests, dramatically reduces the number of "escapes" and allows us to guarantee the AQLs listed below.
	Ship Parts

Here are the QC sample plans used in our A+ test program:

Test	Temperature	AQL
Electrical Functionality Parametric, DC	25°C ) 25°C )	0.035%
Parametric, AC	25°C	0.4%
Electrical Functionality Parametric, DC	At each temperature extreme.	0.05%
Mechanical		
Critical		0.01%
Major		0.28%

#### B+ Program

**B+ Program:** a comprehensive program that assures high quality *and* high reliability of molded integrated circuits.

The B+ program improves both the quality and the reliability of National's digital, linear, and CMOS Epoxy B integrated circuit products. It is intended for the manufacturing user who cannot perform incoming inspection of ICs, or does not wish to do so, yet needs significantly-better-than-usual incoming quality and reliability levels for standard ICs.

Integrated circuit users who specify B+ processed parts will find that the program:

- · Eliminates incoming electrical inspection.
- Eliminates the need for, and thus the added cost of, independent testing laboratories.
- · Reduces the cost of reworking assembed boards.
- · Reduces field failures.
- · Reduces equipment down time.

#### Reliabilty Saves You Money

With the increases population of integrated circuits in modern electronic systems has come an increased concern with IC failures in such systems.

And rightly so, for at least two reasons.

First of all, the effect of component reliability on system reliability can be quite dramatic. For example, suppose that you, as a system manufacturer, were to choose an IC that is 99 percent reliable. You would find that if your system used only 70 such ICs, the overall reliability of the system's IC portion would be only 50 percent. In other words, only one out of two of your systems would operate. The result? A system very costly to produce and probably very difficult to sell.

Secondly, whether the system is large or small you cannot afford to be hounded by the spectre of unnecessary maintenance costs. Not only because labor, repair, and rework costs have risen — and promise to continue to rise — but also because field replacement may be prohibitively expensive. If you ship a system that contains a marginally-performing IC, an IC that later fails in the field, the cost of replacement may be — literally — hundreds of times more than the cost of the failed IC itself.

#### Improving the Reliability of Shipped Parts

The most important factor that affects a part's reliability is its construction: the materials used and the method by which they are assembled.

Now, it's true that reliability cannot be tested into a part. Still, there are tests and procedures that an IC vendor can implement, which will subject the IC to stresses in excess of those that it will endure in actual use, and which will eliminate most marginal, short-life parts.

In any test for reliability the weaker parts will normally fail first. Further, stress tests will accelerate, or shorten, the time to failure of the weak parts. Because the stress tests cause weak parts to fail prior to shipment to the user, the population of shipped parts will in fact demonstrate a higher reliability in use.

#### **Quality Improvement**

When an IC vendor specifies 100 percent final testing of its parts then, in theory, every shipped part should be a good part. However, in any population of mass-produced items there does exist some small percentage of defective parts.

One of the best ways to reduce the number of such faulty parts is, simply, to retest the parts prior to shipment. Thus, if there is a one percent chance that a bad part will escape detection initially, retesting the parts reduces that probability to only 0.01 percent. (A comparable tightening of the QC group's sampled-test plan ensures the maintenance of the improved quality level.)

#### National's B+ Program Gets It All Together

We've stated that the B+ program improves both the quality and the reliability of National's molded integrated circuits, and pointed out the difference between those two concepts. Now, how do we bring them together? The answer is in the B+ program processing, which is a continuum of stress and double testing. With the exception of the final QC inspection, which is sampled, all steps of the B+ process are performed on 100 percent of the program parts. The following flow chart shows how we do it, step by step.

P	SEM Randomly selected wafers are taken from production regularly and subjected to SEM analysis.
	Epoxy B Processing for All Molded Parts At National, all molded semiconductors, including ICs, have been built by this process for some time now. All processing steps, inspections, and QC monitoring are designed to provide highly reliable products. (A reliability report is available that gives, in detail, the background of Epoxy B, the reason for its selection at National, and reliability data that proves its success.)
Ť	Six Hour, 150°C Bake This stress places the die bond and all wire bonds into a combined tensile and shear stress mode, and helps eliminate marginal bonds and electrical connections.
Ť	High Temperature (100°C) Functional Electrical Test A high temperature test such as this with voltages applied places the die under the most severe stress possible. The test is actually performed at 100°C —

30°C higher than the commercial ambient limit. All devices are thoroughly exercised at the 100°C ambient. (Even though Epoxy B processing has virtually eliminated thermal intermittents, we perform this test to ensure against even the remote possibility of such a problem. Remember, the emphasis in the B+ program is on the elimination of those marginally-performing devices that would otherwise lower field reliability of the parts.)

#### **DC** Functional and Parametric Tests

These room-temperature functional and parametric tests are the normal, final tests through which all National products pass.

#### Thermal Shock Monitor

Samples from each package type are selected at random each week and submitted to 100 cycles of liquid to liquid thermal shock -65°C to +150°C. In addition, samples are selected every four weeks and subjected to 2000 temperature cycles of 0°C to +25°C.

#### Tighter-than-normal QC Inspection Plans

Most vendors sample inspect outgoing parts to a 0.3% AQL. When you specify the B+ program, we sample your parts to a 0.035% AQL at room temperature and 0.05% AQL at  $T_A$  Max. This eight times tightening (from 0.3 to 0.035% AQL) coupled with two 100% electrical tests, dramatically reduces the number of "escapes" and allows us to guarantee the AQLs listed below.

Ship Parts

Here are the QC sampling plans used in our B+ test program:

AQL
0.035%
0.4%
0.05%
0.01%

## Advanced Bipolar Logic Data Book Thermal Ratings for IC's

### **Maximum Power Dissipation**

To insure reliable long term operation of its Integrated Circuits, National Semiconductor has specified maximum junction temperature (Tj) limits. These limits are at 150°C for circuits packaged in a molded dual-in-line package (Epoxy B), and 175°C for all other package types.

Maximum power dissipation (PD) of an integrated circuit is limited by maximum allowable junction temperature of the silicon die, and the thermal resistance ( $\theta_J$ - $\chi$ ) of the package. Figure 1 illustrates the relationship between power dissipation and junction temperature.

The line indicating "Maximum Power Rating of Package" is projected from the maximum junction temperature limit (150°C in this example) at a slope corresponding to the package thermal resistance (I/ $\theta$ J- $\chi$ ). Below this line is the safe operating area of the device. Additional constraints are Maximum Power Dissipation and Maximum Operating

Temperature ( $T_A$ ). These parameters may be determined from device data sheets. For this example,  $P_D(MAX) = 300mW$  and  $T_A(MAX) = 70$ °C.

Point "A" in Figure 1 is an operating point corresponding to  $T_A = 50^{\circ}\text{C}$  and  $P_D = 100\text{mW}$ . Determine device junction temperature by projecting a line from point "A" , parallel to the Maximum Power Rating curve, until it intersects the horizontal axis. Tj is determined from the point of intersection with the horizontal axis. For this example, Tj is 45°C.

#### **Thermal Information**

Figure 2 illustrates thermal resistance characteristics for Integrated Circuits packages.

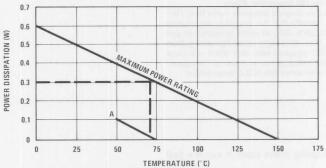


FIGURE 1. Power Dissipation vs Temperature

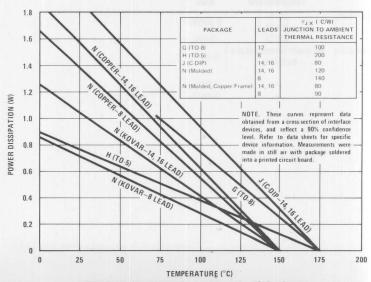
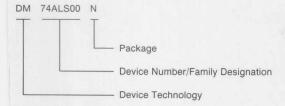


FIGURE 2. Maximum  $\theta_{J-X}$  Values for IC Packages

## **Advanced Bipolar Logic Data Book**

## **Ordering Information**

Ordering information for National Devices is covered in this catalogue as follows



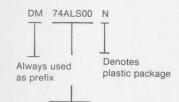
## **Device Technology**

■ DM—Digital Monolithic

#### **Device Number**

- 4 to 8 digit number
- 1st two digits denote temperature selection 54—denotes full mil range specification −55°C to +125°C
- 74—denotes commercial specification 0°C to 70°C

Example: How to order



Commercial temp range function found in the 54/74ALS family

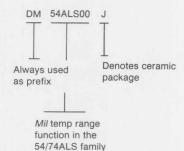
## **Family Designation**

- 54/74ALSXX(X)—Advanced Low Power Schottky
- 54/74ASXX(X)—Advanced Schottky

National Semiconductor manufactures a complete line of industry standard logic products. The industry standard number identifying a particular function is used in marking the product with the only difference being prefixes and suffixes noted above.

When ordering a particular product, please specify the entire number, including the *DM prefix* and appropriate *package* suffix. This will help in processing your order more quickly.

Note: Although the *part* number is generally uniform throughout the industry, competitors vary in terms of denoting package type and temperature selection. Please refer to the industry cross reference guide in the back of this data book for properly cross referencing competitor products.



# Advanced Low Power Schottky

The DM54/74ALS family of devices are designed to meet the needs of system designers requiring very low power, higher low level threshold than LS and toggle capability up to 100 MHz. In addition ALS features a 40% reduction in propagation delay times of present LS functions (4ns per gate) while reducing power levels by half (1mw per gate).

In addition to speed improvements, higher threshold, and very low power, the ALS family offers direct TTL/LS replacement functions, ideal for system upgrades and new system designs.

For maximum design flexibility and elimination of special drawings, the ALS family will be introduced with  $\pm$  10% V<sub>CC</sub> over the military and commercial full temp range as standard product. Furthermore, all switching characteristics are guaranteed over the full temperature and V<sub>CC</sub> range.



This DNS-YV-EAL C Territor of devices are developed to what it is expense and properly well and properly and

In addition to speed improvements, higher threshold, and viny ten power, the AUS family allies direct TTLLS replacement functions, little that the upgradies and now mystem dissigns.

Formsteinem design hestallly and dimination of exceld drawings, the ALS family will be introduced with at 10% VCC even the militar card committee of the lamp rates be statistical product. Furthermore, at swipping drampter are guaranteed over the Lating and the VCC range.



## ADVANCED LOW POWER SCHOTTKY

### **Absolute Maximum Ratings** (Note 1)

Supply Voltage, V<sub>CC</sub> (1) Input Voltage, V<sub>I</sub>: All Inputs 7V 7V I/O Ports 5.5V Off State (High Level) Voltage Applied to Open-Collector Outputs 7V 5.5V

High Level Voltage Applied to 3-State Outputs Operating Free-Air Temperature Range:

SN54ALS -55°C to 125°C SN74ALS 0°C to 70°C

Storage Temperature Range -65°C to 150°C

## **Recommended Operating Conditions**

		Star	ndard Ou	utput	Bu	iffer Out	put	Bus	Driver O	utput	
Parameter		Min	Nom	<b>Max</b> 5.5	Min	<b>Nom</b> 5.0	<b>Max</b> 5.5	Min 4.5	<b>Nom</b> 5.0	<b>Max</b> 5.5	Unit
Supply Voltage	54/74ALS	4.5	5.0		4.5						
High Level Input Voltage, VIH	54/74ALS	2.0			2.0			2.0			V
Low Level Input Voltage, V <sub>IL</sub>	54/74ALS			0.8			0.8			0.8	V
High Level Output	54ALS			-0.4			-1			-12	mA
Voltage, IOH (2)	74ALS			-0.4			-2.6			-15	mA
High Level Output Current, VOH (3)	54/74ALS			5.5			5.5			5.5	V
Low Level Output	54/74ALS			4			12			12	mA
Current, IOL	74ALS	64	4番	8			24			24/48	mA
Operating Free-Air	54ALS	-55		125	-55		125	-55		125	°C
Temperature, TA	74ALS	0	12	70	0		70	0		70	°C

**Electrical Characteristics** over recommended operating free air temperature range (unless otherwise noted)

				Star	dard Ou	tput	Bu	Buffer Output			Bus Driver Output		
	Parameter	Conditions		Min	Typ(4)	Max	Min	Typ(4)	Max	Min	Typ(4)	Max	Unit
VIK	Input Clamp Voltage	$V_{CC} = 4.5V$ $I_{I} = -18\text{mA}$				-1.5			-1.5			-1.5	٧
VOH	High Level Output	V <sub>CC</sub> = 4.5V, I <sub>C</sub>	DH = MAX				2.4	3.2		2	3.2		V
	Voltage (2)	V <sub>CC</sub> = 4.5V, I <sub>C</sub>	$_{\rm DH} = -3$ mA							2.4	3.2		V
		$I_{OH} = -0.4$ mA	1	V <sub>CC</sub> -2V			V <sub>CC</sub> -2V			V <sub>CC</sub> -2V			V
ЮН	High Level Output Current (3)	$V_{CC} = 4.5V$ $V_{OH} = 5.5V$				0.1			0.1			0.1	mA
VOL	Low Level Output Voltage	$V_{CC} = 4.5V$	74ALS		0.35	0.5		0.35	0.5		0.35	0.5	V
		I <sub>OL</sub> = MAX	54/74ALS		0.25	0.4		0.25	0.4		0.25	0.4	V
lı	Input Current at Maximum Input Voltage	$V_{CC} = 5.5V$ $V_{I} = 7V$				0.1			0.1			0.1	mA
ΊΗ	High Level Input Current	$V_{CC} = 5.5V$ $V_{I} = 2.7V$				20			20		9.5	20	μΑ
ΊL	Low Level Input Current	$V_{CC} = 5.5V$ $V_{IL} = 0.4V$			-0.02	-0.2		-0.05	-0.2		-0.05	-0.2	mA
10	Output Current (5)	$V_{CC} = 5.5V$ $V_{O} = 2.25V$		-30		-110	-30		-110	-30		-110	mA
lozh	Off-State Output Current, High Level Voltage Applied (6)	$V_{CC} = 5.5V$ $V_{O} = 2.7V$							20			20	μΑ
lozL	Off-State Output Current,	$V_{CC} = 5.5V$	I/O Ports	101					-0.2	FORE		-0.2	mA
	Low Level Voltage Applied (6)	$V_O = 0.4V$	Non-I/O						-20			-20	μΑ
Icc	Supply Current (7)	$V_{CC} = 5.5V$								- 11.5			mA

NOTE 1: Voltage values are with respect to network ground terminal.

NOTE 2: Does not apply to open-collector outputs.

NOTE 3: Applies only to open-collector outputs.

NOTE 4: All typical numbers are at  $V_{CC} = 5V$ ,  $T_A = 25$ °C.

NOTE 5: The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current, IOS.

NOTE 6: Applies only to TRI-STATE outputs.

NOTE 7: Refer to individual data sheet for ICC limits.



## DM54ALS00/DM74ALS00 Quad 2-Input NAND Gates

#### **Features**

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

## **Absolute Maximum Ratings**

Supply Voltage Input Voltage Operating Free Air Temperature Range

DM54ALS DM74ALS

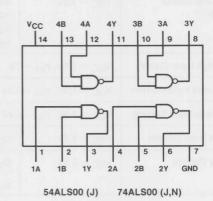
Storage Temperature Range

7V 7V

-55°C to 125°C 0°C to 70°C -65°C to 150°C

## **Connection Diagram**

 $Y = \overline{AB}$ 



		1					
Parameter	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, V <sub>CC</sub>	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, VIH	2			2			٧
Low Level Input Voltage, V <sub>IL</sub>			0.8	Market State Service		0.8	V
High Level Output Current, IOH	March Topics	1111	-0.4	multi me		-0.4	mA
Low Level Output Current, IOL		pulsan	4	mil and		8	mA

## Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Voltage	$V_{CC} = 4.5V, I_{I} = -18 \text{ mA}$				-1.5	٧
Vон	High Level Output Voltage	$I_{OH} = -0.4$ mA		V <sub>CC</sub> -2	di no	intro	V
VOL	Low Level Output Voltage	V <sub>CC</sub> = 4.5V	54/74ALS I <sub>OL</sub> = 4 mA		0.25	0.4	V
			74ALS I <sub>OL</sub> = 8 mA		0.35	0.5	V
lį	Max High Input Current	$V_{CC} = 5.5V, V_{IH}$			0.1	mA	
ΊΗ	High Level Input Current	$V_{CC} = 5.5V, V_{IH}$	= 2.7V	Tal. o		20	μΑ
IIL	Low Level Input Current	$V_{CC} = 5.5V, V_{IL}$	= 0.4V			-0.2	mA
IO	Output Drive Current	$V_{CC} = 5.5V$	V <sub>O</sub> = 2.25V	-30		-110	mA
ICC	Supply Current	$V_{CC} = 5.5V$	Outputs High		0.43	0.85	mA
				1.62	3.0	mA	

## Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions		M54ALS	00		7		
		Min	Тур	Max	Min	Тур	Max	Unit
TPLH, Propagation delay time. Low to high level output	$V_{CC} = 4.5 \text{ to } 5.5V$ $R_L = 500 \Omega,$ $C_L = 50 \text{pF}.$	2	4	10	2	4	9	ns
TPHL, Propagation delay time. High to low level output		2	4	10	2	4	9	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-1.

# DM54ALS01/DM74ALS01 Quad 2-Input NAND Gates with Open Collector Outputs

#### **Features**

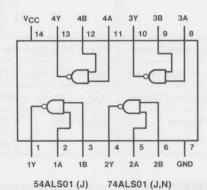
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

## **Absolute Maximum Ratings**

Supply Voltage	7V
Input Voltage	7V
Off State (High Level)	7V
Output Voltage	
Operating Free Air Temperature Range	
DM54ALS	-55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	-65°C to 150°C

## **Connection Diagram**

 $Y = \overline{AB}$ 



ligh Level Input Voltage, VIH		DM54ALS01			M74ALS0	1	
	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, V <sub>CC</sub>	4.5	5	5.5	4.5	5	5.5	٧
High Level Input Voltage, VIH	2		-	2			V
Low Level Input Voltage, VIL	Messal		0.8			0.8	V
High Level Output Voltage, VOH	are in the		5.5	na orbin		5.5	V
Low Level Output Current, IOL	-O strakt EC		4		Na Maria	8	mA

## Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Voltage	V <sub>CC</sub> = 4.5V, I <sub>I</sub> =	-18 mA	,ettiqui?	12003 (20)	-1.5	V
ЮН	High Level Output Current	V <sub>CC</sub> = 4.5V V <sub>OH</sub> = 5.5V		mierz		100	μΑ
VOL Low Level Output Voltage	V <sub>CC</sub> = 4.5V	54/74ALS I <sub>OL</sub> = 4 mA		0.25	0.4	٧	
	at m va	7 7 7 3	74ALS I <sub>OL</sub> = 8 mA		0.35	0.5	V
l <sub>l</sub>	Max High Input Current	V <sub>CC</sub> = 5.5V, V <sub>IH</sub>	= 7V			0.1	mA
Ιн	High Level Input Current	$V_{CC} = 5.5V, V_{IH}$	= 2.7V			20	μΑ
IIL	Low Level Input Current	$V_{CC} = 5.5V, V_{IL}$	= 0.4V			-0.2	mA
Icc	Supply Current	$V_{CC} = 5.5V$	Outputs High		0.43	0.85	mA
			Outputs Low		1.62	3.0	mA

## Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter		DM54ALS01			0			
	Conditions	Min	Тур	Max	Min	Тур	Max	ns
TPLH, Propagation delay time. Low to high level output	$V_{CC} = 4.5 \text{ to } 5.5V$ $R_L = 2K \Omega$ , $C_L = 50 \text{ pF}$ .	23	27	59	23	27	54	ns
TPHL, Propagation delay time. High to low level output		4	7	25	4	7	20	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-4.

## DM54ALS02/DM74ALS02 Quad 2-Input NOR Gates

#### **Features**

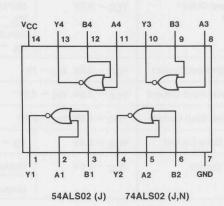
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

## **Absolute Maximum Ratings**

Cumply Voltage	7V
Supply Voltage Input Voltage	7 V
Operating Free Air Temperature Range	The same of the sa
DM54ALS	-55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	-65°C to 150°C

## **Connection Diagram**

 $Y = \overline{A + B}$ 



ligh Level Input Voltage, VIH	1	DM54ALS02			DM74ALS0	2	
	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, VCC	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, VIH	2			2			٧
Low Level Input Voltage, VIL			0.8	A STATE OF		0.8	٧
High Level Output Current, IOH	politic le transcription	m/ft,	-0.4	amo	muless	-0.4	mA
Low Level Output Current, IOL		potentia	4	Hol Lin	all-down	8	mA

## Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Voltage	V <sub>CC</sub> = 4.5V, I <sub>I</sub> =	-18 mA			-1.5	V
Vон	High Level Output Voltage	$I_{OH} = -0.4$ mA		V <sub>CC</sub> -2		dnys	V
VOL Low Level Output Voltage		V <sub>CC</sub> = 4.5V	54/74ALS I <sub>OL</sub> = 4 mA		0.25	0.4	V
	a a ori	74ALS I <sub>OL</sub> = 8 mA	0.35	0.5	V		
Ц	Max High Input Current	$V_{CC} = 5.5V, V_{IH}$	= 7V			0.1	mA
ΊΗ	High Level Input Current	$V_{CC} = 5.5V, V_{IH}$	= 2.7V	1144		20	μΑ
IIL	Low Level Input Current	$V_{CC} = 5.5V, V_{IL}$	= 0.4V			-0.2	mA
IO	Output Drive Current	$V_{CC} = 5.5V$	V <sub>O</sub> = 2.25V	-30		-110	mA
ICC	Supply Current	$V_{CC} = 5.5V$	Outputs High		0.85	2.2	mA
			Outputs Low		2.16	4.0	mA

## Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter		DM54ALS02			DM74ALS02			I I with
	Conditions	Min	Тур	Max	Min	Тур	Max	Unit
TPLH, Propagation delay time. Low to high level output	$V_{CC} = 4.5 \text{ to } 5.5V$ $R_L = 500  \Omega$ , $C_L = 50  \text{pF}$ .	2	5	11	2	5	10	ns
TPHL, Propagation delay time. High to low level output		2	5	10	2	5	9	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-1.

# DM54ALS03/DM74ALS03 Quad 2-Input NAND Gates with Open Collector Outputs

#### **Features**

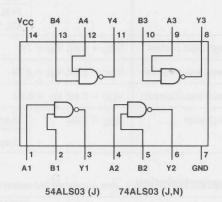
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

## **Absolute Maximum Ratings**

Supply Voltage	7V
Input Voltage	7V
Off State (High Level)	
Output Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	-55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	-65°C to 150°C

### **Connection Diagram**

 $Y = \overline{AB}$ 



	1	DM54ALS03			DM74ALS0		
	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, V <sub>CC</sub>	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, VIH	2		3 70	2			V
Low Level Input Voltage, VIL			0.8			0.8	V
High Level Output Voltage, VOH	Heliquid II		5.5			5.5	V
Low Level Output Current, IOL			4	WOD ex		8	mA

## **Electrical Characteristics** over recommended operating free air temperature range (Note 1)

	Parameter	Conditions	Min	Тур	Max	Unit	
VIK	Input Clamp Voltage	V <sub>CC</sub> = 4.5V, I <sub>I</sub> =	-18 mA	hokest		-1.5	٧
ЮН	High Level Output Current	$V_{CC} = 4.5V, V_{OF}$	H = 5.5V			100	μΑ
VOL Low Level Output Voltage	$V_{CC} = 4.5V$	54/74ALS I <sub>OL</sub> = 4 mA		0.25	0.4	٧	
	W 45 mg		74ALS I <sub>OL</sub> = 8 mA		0.35	0.5	V
l <sub>l</sub>	Max High Input Current	$V_{CC} = 5.5V, V_{IH}$	= 7V			0.1	mA
IIH	High Level Input Current	$V_{CC} = 5.5V, V_{IH}$	= 2.7V			20	μΑ
IIL	Low Level Input Current	$V_{CC} = 5.5V, V_{IL}$	= 0.4V	MA -		-0.2	mA
ICC	Supply Current	$V_{CC} = 5.5V$	Outputs High		0.43	0.85	mA
			Outputs Low		1.62	3.0	mA

## Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter			DM54ALS03			DM74ALS03		
	Conditions	Min	Тур	Max	Min	Тур	Max	ns
TPLH, Propagation delay time. Low to high level output	$V_{CC} = 4.5 \text{ to } 5.5V$ $R_{L} = 2K \Omega$ , $C_{L} = 50 \text{ pF}$ .	23	27	59	23	27	54	ns
TPHL, Propagation delay time. High to low level output		4	7	25	4	7	20	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-4.



## DM54ALS04/DM74ALS04 Hex Inverters

#### **Features**

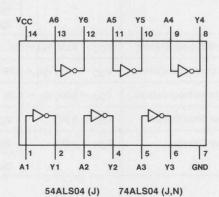
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

## **Absolute Maximum Ratings**

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	-55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	-65°C to 150°C

## **Connection Diagram**

 $Y = \overline{A}$ 



	DM54ALS04			1			
Parameter	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, V <sub>CC</sub>	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, VIH	2			2			٧
Low Level Input Voltage, VIL			0.8	ATT OF THE		0.8	V
High Level Output Current, IOH	mich paris Con	E-Park	-0.4		Mellay.	-0.4	mA
Low Level Output Current, IOL		- junto sil	4	eren dan	र शिवडारी	8	mA

## Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Voltage	$V_{CC}=4.5V$ , $I_{I}=-18$ mA				-1.5	V
Vон	High Level Output Voltage	$I_{OH} = -0.4$ mA		V <sub>CC</sub> -2			٧
VOL	Low Level Output Voltage	$V_{CC} = 4.5V$	54/74ALS I <sub>OL</sub> = 4 mA		0.25	0.4	٧
	S 07 TH	74ALS I <sub>OL</sub> = 8 mA		0.35	0.5	٧	
lį	Max High Input Current	V <sub>CC</sub> = 5.5V, V <sub>IH</sub> = 7V				0.1	mA
ΙΗ	High Level Input Current	$V_{CC} = 5.5V, V_{IH}$	= 2.7V			20	μΑ
IIL	Low Level Input Current	$V_{CC} = 5.5V, V_{IL}$	= 0.4V			-0.2	mA
IO	Output Drive Current	$V_{CC} = 5.5V$	$V_0 = 2.25V$	-30		-110	mA
Icc	Supply Current	$V_{CC} = 5.5V$	Outputs High		0.65	1.1	mA
	000 21 70		Outputs Low		2.4	3.8	mA

## Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter		DM54ALS04						
	Conditions	Min	Тур	Max	Min	Тур	Max	Unit
TPLH, Propagation delay time. Low to high level output	$V_{CC} = 4.5 \text{ to } 5.5V$ $R_L = 500  \Omega$ , $C_L = 50  \text{pF}$ .	2	4	10	2	4	9	ns
TPHL, Propagation delay time. High to low level output		2	4	9	2	4	8	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-1.

-65°C to 150°C

## DM54ALS05/DM74ALS05 Hex Inverters with Open Collector Outputs

#### **Features**

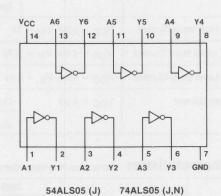
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and VCC Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

## **Absolute Maximum Ratings**

Supply Voltage	7V
Input Voltage	7V
Off State (High Level)	7V
Output Voltage	
Operating Free Air Temperature Range	
DM54ALS	-55°C to 125°C
DM74ALS	0°C to 70°C

### **Connection Diagram**





Storage Temperature Range

	1	OM54ALS0	5	1			
Parameter	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, VCC	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, VIH	2			2			V
Low Level Input Voltage, VIL	ola la el a		0.8			0.8	V
High Level Output Voltage, VOH	av es e		5.5	denan	- in the	5.5	V
Low Level Output Current, IOL	and and a		4	SEPTIME TO SEPTIME	Market S	8	mA

## Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Voltage	$V_{CC} = 4.5V$ , $I_{I} = -18$ mA		a)magnish		-1.5	V
ЮН	High Level Output Current	$V_{CC} = 4.5V, V_{OH}$	H = 5.5V			100	μΑ
VOL	Low Level Output Voltage	V <sub>CC</sub> = 4.5V	54/74ALS I <sub>OL</sub> = 4 mA		0.25	0.4	V
		74ALS I <sub>OL</sub> = 8 mA		0.35	0.5	٧	
IJ	Max High Input Current	$V_{CC} = 5.5V, V_{IH}$	= 7V			0.1	mA
ΊΗ	High Level Input Current	$V_{CC} = 5.5V, V_{IH}$	= 2.7V			20	μΑ
IIL	Low Level Input Current	V <sub>CC</sub> = 5.5V, V <sub>IL</sub> = 0.4V				-0.2	mA
ICC	Supply Current	$V_{CC} = 5.5V$	Outputs High		0.65	1.1	mA
			Outputs Low		2.4	3.8	mA

## Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	PER LIBERTAN ILLUSTRA	DM54ALS05				DM74ALS05			
	Conditions	Min	Тур	Max	Min	Тур	Max	Unit	
TPLH, Propagation delay time. Low to high level output	$V_{CC} = 4.5 \text{ to } 5.5V$ $R_L = 2K \Omega$ , $C_L = 50 \text{ pF}$ .	23	27	59	23	27	54	ns	
TPHL, Propagation delay time. High to low level output		4	7	24	4	7	19	ns	

NOTE 1: See notes pg. 1-iii, figures pg. 3-4.

## DM54ALS08/DM74ALS08 Quad 2-Input AND Gates

#### **Features**

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

## **Absolute Maximum Ratings**

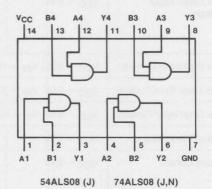
Supply Voltage
Input Voltage
Operating Free Air Temperature Range
DM54ALS
DM74ALS

DM74ALS 0°C to 70°C
Storage Temperature Range -65°C to 150°C

-55°C to 125°C 0°C to 70°C

## **Connection Diagram**

Y = AB



	DM54ALS08				Marie 1		
Parameter	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, VCC	4.5	5	5.5	4.5	5	5.5	٧
High Level Input Voltage, VIH	2			2			٧
Low Level Input Voltage, VIL			0.8	lette ens	saudier.	0.8	٧
High Level Output Current, IOH		Ruite	-0.4		SAME	-0.4	mA
Low Level Output Current, IOL		yelseniss	4	HBL BAU	NSF-11	8	mA

## Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Voltage	$V_{\rm CC}=4.5V$ , $I_{ m I}=-18$ mA				-1.5	V
Vон	High Level Output Voltage	$I_{OH} = -0.4$ mA		V <sub>CC</sub> -2		110	V
VOL	Low Level Output Voltage	V <sub>CC</sub> = 4.5V	54/74ALS I <sub>OL</sub> = 4 mA		0.25	0.4	٧
4 4 11 11 11		74ALS I <sub>OL</sub> = 8 mA		0.35	0.5	V	
lį —	Max High Input Current	$V_{CC} = 5.5V, V_{IH} = 7V$				0.1	mA
ΙΗ	High Level Input Current	$V_{CC} = 5.5V, V_{IH}$	= 2.7V			20	μΑ
ŊĽ	Low Level Input Current	$V_{CC} = 5.5V, V_{IL}$	= 0.4V			-0.2	mA
10	Output Drive Current	$V_{CC} = 5.5V$	$V_0 = 2.25V$	-30		-110	mA
ICC	Supply Current	$V_{CC} = 5.5V$	Outputs High		1.3	2.4	mA
	physical property and party and part	A DEMI	Outputs Low		2.2	4.0	mA

## Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter		DM54ALS08						
	Conditions	Min	Тур	Max	Min	Тур	Max	Unit
TPLH, Propagation delay time. Low to high level output	$V_{CC} = 4.5 \text{ to } 5.5V$ $R_L = 500 \Omega,$ $C_L = 50 \text{pF}.$	3	5	13	3	5	12	ns
TPHL, Propagation delay time. High to low level output		3	5	11	3	5	10	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-1.

# DM54ALS09/DM74ALS09 Quad 2-Input AND Gates with Open Collector Outputs

#### **Features**

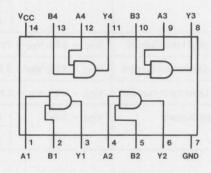
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

### **Absolute Maximum Ratings**

Supply Voltage	7V
Input Voltage	7V
Off State (High Level)	
Output Voltage	7V
Operating Free Air Temperature R	ange
DM54ALS	-55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	-65°C to 150°C

## **Connection Diagram**

Y = AB



54ALS09 (J) 74ALS09 (J,N)

	DM54ALS09			DM74ALS09			Ma I
Parameter	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, VCC	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, VIH	2			2			V
Low Level Input Voltage, VIL			0.8			0.8	V
High Level Output Voltage, VOH			5.5	ag Jinesii		5.5	V
Low Level Output Current, IOL			4			8	mA

## **Electrical Characteristics** over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Voltage	$V_{CC} = 4.5V$ , $I_{I} = -18$ mA				-1.5	V
ЮН	High Level Output Current	$V_{CC} = 4.5V, V_{OR}$	H = 5.5V			100	μΑ
VOL	Low Level Output Voltage	$V_{CC} = 4.5V$	54/74ALS I <sub>OL</sub> = 4 mA		0.25	0.4	٧
			74ALS I <sub>OL</sub> = 8 mA		0.35	0.5	V
l <sub>F</sub>	Max High Input Current	$V_{CC} = 5.5V, V_{IH}$	= 7V			0.1	mA
ΙΗ	High Level Input Current	V <sub>CC</sub> = 5.5V, V <sub>IH</sub>	= 2.7V			20	μΑ
I <sub>I</sub> L	Low Level Input Current	$V_{CC} = 5.5V, V_{IL}$	= 0.4V			-0.2	mA
ICC	Supply Current	$V_{CC} = 5.5V$	Outputs High		1.3	2.4	mA
			Outputs Low		2.2	4.0	mA

## Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54ALS09			DM74ALS09			
		Min	Тур	Max	Min	Тур	Max	Unit
TPLH, Propagation delay time. Low to high level output	$V_{CC} = 4.5 \text{ to } 5.5V$ $R_{L} = 2K \Omega$ , $C_{L} = 50 \text{ pF}$ .	23	27	59	23	27	54	ns
TPHL, Propagation delay time. High to low level output		4	7	14	4	7	13	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-4.



## DM54ALS10/DM74ALS10 Triple 3-Input NAND Gates

#### **Features**

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

### **Absolute Maximum Ratings**

 Supply Voltage
 7V

 Input Voltage
 7V

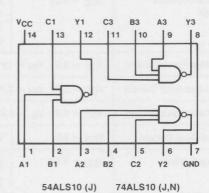
 Operating Free Air Temperature Range
 —55°C to 125°C

 DM54ALS
 —0°C to 70°C

 Storage Temperature Range
 —65°C to 150°C

## **Connection Diagram**

 $Y = \overline{ABC}$ 



	DM54ALS10			DM74ALS10			
Parameter	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, VCC	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, VIH	2			2			٧
Low Level Input Voltage, VIL			0.8			0.8	V
High Level Output Current, IOH		N. Pi	-0.4			-0.4	mA
Low Level Output Current, IOL		i man	4	idgi jbeti		8	mA

## Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Voltage	$V_{CC} = 4.5V, I_{I} =$	-18 mA			-1.5	٧
Vон	High Level Output Voltage	$I_{OH} = -0.4$ mA		V <sub>CC</sub> -2		ar in	V
VOL	Low Level Output Voltage	V <sub>CC</sub> = 4.5V	54/74ALS I <sub>OL</sub> = 4 mA		0.25	0.4	V
	4 1 1 16		74ALS I <sub>OL</sub> = 8 mA		0.35	0.5	V
lį	Max High Input Current	$V_{CC} = 5.5V, V_{IH} = 7V$				0.1	mA
I <sub>IH</sub>	High Level Input Current	$V_{CC} = 5.5V, V_{IH}$	= 2.7V	503		20	μΑ
IIL	Low Level Input Current	$V_{CC} = 5.5V, V_{IL}$	= 0.4V			-0.2	mA
10	Output Drive Current	$V_{CC} = 5.5V$	$V_0 = 2.25V$	-30		-110	mA
Icc	Supply Current	$V_{CC} = 5.5V$	Outputs High		0.32	0.6	mA
			Outputs Low		1.2	2.2	mA

## Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54ALS10			DM74ALS10			
		Min	Тур	Max	Min	Тур	Max	Unit
TPLH, Propagation delay time. Low to high level output	$V_{CC} = 4.5 \text{ to } 5.5V$ $R_L = 500 \Omega,$ $C_L = 50 \text{pF}.$	2	4	10	2	4	9	ns
TPHL, Propagation delay time. High to low level output		2	6	14	2	6	12	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-1.



## DM54ALS11/DM74ALS11 Triple 3-Input AND Gates

#### **Features**

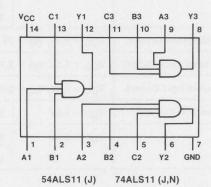
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

## **Absolute Maximum Ratings**

Supply Voltage	7\
Input Voltage	7\
Operating Free Air Temperature Range	
DM54ALS	-55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	-65°C to 150°C

## **Connection Diagram**

Y = ABC



	1	DM54ALS11			DM74ALS11			
Parameter	Min	Nom	Max	Min	Nom	Max	Unit	
Supply Voltage, V <sub>CC</sub>	4.5	5	5.5	4.5	5	5.5	V	
High Level Input Voltage, VIH	2			2			٧	
Low Level Input Voltage, VIL			0.8			0.8	V	
High Level Output Current, IOH		i min	-0.4			-0.4	mA	
Low Level Output Current, IOL		THE RES	4	nol tale		8	mA	

## Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Voltage	$V_{CC} = 4.5V$ , $I_I =$	-18 mA			-1.5	V
Vон	High Level Output Voltage	$I_{OH} = -0.4$ mA		V <sub>CC</sub> -2		0 0	٧
VOL	Low Level Output Voltage	V <sub>CC</sub> = 4.5V	54/74ALS I <sub>OL</sub> = 4 mA		0.25	0.4	V
6 0 5		74ALS I <sub>OL</sub> = 8 mA		0.35	0.5	V	
ΙĮ	Max High Input Current	$V_{CC} = 5.5V, V_{IH}$	$V_{CC} = 5.5V, V_{IH} = 7V$			0.1	mA
lіН	High Level Input Current	$V_{CC} = 5.5V, V_{IH}$	= 2.7V			20	μΑ
IIL	Low Level Input Current	$V_{CC} = 5.5V, V_{IL}$	= 0.4V			-0.2	mA
IO	Output Drive Current	$V_{CC} = 5.5V$	$V_0 = 2.25V$	-30		-110	mA
ICC		$V_{CC} = 5.5V$	Outputs High		1.0	1.8	mA
			Outputs Low		1.6	3.0	mA

## Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54ALS11						
		Min	Тур	Max	Min	Тур	Max	Unit
TPLH, Propagation delay time. Low to high level output	$V_{CC} = 4.5 \text{ to } 5.5V$ $R_L = 500 \Omega$ , $C_L = 50 \text{ pF}$ .	3	5	17	3	5	15	ns
TPHL, Propagation delay time. High to low level output		3	6	11	3	6	10	ns



## DM54ALS12/DM74ALS12 Triple 3-Input NAND Gates with Open Collector Outputs

#### **Features**

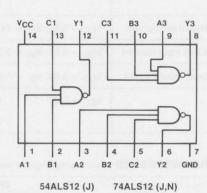
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

### **Absolute Maximum Ratings**

Supply Voltage	7V
Input Voltage	7V
Off State (High Level)	
Output Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	-55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Bange	-65°C to 150°C

#### **Connection Diagram**

 $Y = \overline{ABC}$ 



	DM54ALS12			1			
Parameter	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, VCC	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, VIH	2		Page	2	HAR		V
Low Level Input Voltage, VIL			0.8			0.8	V
High Level Output Voltage, VOH			5.5	Talk Loo	hestury :	5.5	V
Low Level Output Current, IOL	nest for L L.		4			8	mA

## Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Voltage	V <sub>CC</sub> = 4.5V, I <sub>I</sub> =	-18 mA	J. Prophysics		-1.5	V
ЮН	High Level Output Current	$V_{CC} = 4.5V, V_{OI}$	H = 5.5V			100	μΑ
VOL	Low Level Output Voltage	$V_{CC} = 4.5V$	54/74ALS I <sub>OL</sub> = 4 mA	NI PURE	0.25	0.4	٧
			74ALS I <sub>OL</sub> = 8 mA		0.35	0.5	V
l <sub>I</sub>	Max High Input Current	$V_{CC} = 5.5V, V_{IH}$	= 7V			0.1	mA
ΙΗ	High Level Input Current	V <sub>CC</sub> = 5.5V, V <sub>IH</sub>	= 2.7V			20	μΑ
IIL	Low Level Input Current	$V_{CC} = 5.5V, V_{IL}$	= 0.4V			-0.2	mA
ICC		$V_{CC} = 5.5V$	Outputs High		0.32	0.6	mA
			Outputs Low		1.2	2.2	mA

## Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54ALS12						
		Min	Тур	Max	Min	Тур	Max	Unit
TPLH, Propagation delay time. Low to high level output	$V_{CC} = 4.5 \text{ to } 5.5 \text{V}$ $R_L = 500 \Omega,$ $C_L = 50 \text{pF}.$	23	27	54	23	27	59	ns
TPHL, Propagation delay time. High to low level output		5	8	29	5	8	23	ns



# DM54ALS15/DM74ALS15 Triple 3-Input AND Gates with Open Collector Outputs

#### **Features**

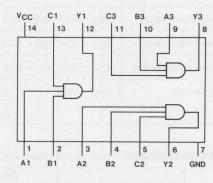
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

#### **Absolute Maximum Ratings**

Supply Voltage	7V
Input Voltage	7V
Off State (High Level)	
Output Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	-55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	-65°C to 150°C

#### **Connection Diagram**

Y = ABC



54ALS15 (J) 74ALS15 (J,N)

	1	DM54ALS1	5				
Parameter	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, VCC	4.5	5	5.5	4.5	5	5.5	٧
High Level Input Voltage, VIH	2	udilla	2 70	2		i i	V
Low Level Input Voltage, VIL			0.8			0.8	V
High Level Output Voltage, VOH			5.5			5.5	٧
Low Level Output Current, IOL		- Albert	4	shall me		8	m.A

## **Electrical Characteristics** over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Voltage	V <sub>CC</sub> = 4.5V, I <sub>I</sub> =	-18 mA	III SATE		-1.5	V
ЮН	High Level Output Current	$V_{CC} = 4.5V, V_{OH}$	$V_{CC} = 4.5V, V_{OH} = 5.5V$			100	μΑ
VOL	Low Level Output Voltage	V <sub>CC</sub> = 4.5V	54/74ALS I <sub>OL</sub> = 4 mA		0.25	0.4	V
			74ALS I <sub>OL</sub> = 8 mA		0.35	0.5	٧
lį	Max High Input Current	$V_{CC} = 5.5V, V_{IH}$	= 7V			0.1	mA
Ιн	High Level Input Current	V <sub>CC</sub> = 5.5V, V <sub>IH</sub>	= 2.7V			20	μΑ
IIL	Low Level Input Current	$V_{CC} = 5.5V, V_{IL}$	= 0.4V			-0.2	mA
ICC	Supply Current	$V_{CC} = 5.5V$	Outputs High	-01	1.0	1.8	mA
			Outputs Low		1.66	3.0	mA

## Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54ALS15						
		Min	Тур	Max	Min	Тур	Max	Unit
T <sub>PLH</sub> , Propagation delay time. Low to high level output	$V_{CC} = 4.5 \text{ to } 5.5V$ $R_{L} = 2K \Omega$ , $C_{L} = 50 \text{ pF}$ .	23	27	59	23	27	54	ns
TPHL, Propagation delay time. High to low level output		4	7	14	4	7	13	ns

## DM54ALS20/DM74ALS20 Dual 4-Input NAND Gates

#### **Features**

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

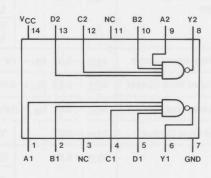
#### **Absolute Maximum Ratings**

Supply Voltage 7V
Input Voltage 7V
Operating Free Air Temperature Range
DM54ALS -55°C to 125°C

 $\begin{array}{ccc} {\rm DM74ALS} & {\rm 0^{\circ}C~to~70^{\circ}C} \\ {\rm Storage~Temperature~Range} & -65^{\circ}C~to~150^{\circ}C \end{array}$ 

## **Connection Diagram**

 $Y = \overline{ABCD}$ 



54ALS20 (J) 74ALS20 (J,N)

	DM54ALS20						
Parameter	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, V <sub>CC</sub>	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, VIH	2			2			V
Low Level Input Voltage, VIL			0.8			0.8	V
High Level Output Current, IOH			-0.4	ord the edu Supplier of the		-0.4	mA
Low Level Output Current, IOL			4			8	mA

## Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Voltage	V <sub>CC</sub> = 4.5V, I <sub>I</sub> =	-18 mA			-1.5	V
Vон	High Level Output Voltage	$I_{OH} = -0.4$ mA		V <sub>CC</sub> -2		April 19	V
VOL	Low Level Output Voltage	V <sub>CC</sub> = 4.5V	54/74ALS I <sub>OL</sub> = 4 mA		0.25	0.4	V
			74ALS I <sub>OL</sub> = 8 mA		0.35	0.5	V
II	Max High Input Current	$V_{CC} = 5.5V, V_{IH}$	$V_{CC} = 5.5V, V_{IH} = 7V$			0.1	mA
ΊΗ	High Level Input Current	$V_{CC} = 5.5V, V_{IH}$	= 2.7V	9351		20	μΑ
IIL	Low Level Input Current	$V_{CC} = 5.5V, V_{IL}$	= 0.4V			-0.2	mA
IO	Output Drive Current	$V_{CC} = 5.5V$	V <sub>O</sub> = 2.25V	-30		-110	mA
ICC	GO H THE	$V_{CC} = 5.5V$	Outputs High		0.22	0.4	mA
		and the sales	Outputs Low		0.81	1.5	mA

## Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter		DM54AL\$20				M74ALS2	20	
	Conditions	Min	Тур	Max	Min	Тур	Max	Unit
TPLH, Propagation delay time. Low to high level output	$V_{CC} = 4.5 \text{ to } 5.5V$ $R_L = 500  \Omega,$ $C_L = 50  \text{pF}.$	2	4	10	2	4	9	ns
TPHL, Propagation delay time. High to low level output		5	9	17	5	9	15	ns

## DM54ALS21/DM74ALS21 Dual 4-Input AND Gates

#### **Features**

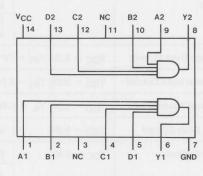
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

#### **Absolute Maximum Ratings**

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	-55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	-65°C to 150°C

#### **Connection Diagram**

Y = ABCD



54ALS21 (J) 74ALS21 (J,N)

		DM54ALS2	21		1		
Parameter	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, VIH	2			2			V
Low Level Input Voltage, VIL			0.8			0.8	V
High Level Output Current, IOH	Light	141	-0.4		Support	-0.4	mA
Low Level Output Current, IOL		T-price	4		MON-EL	8	mA

## **Electrical Characteristics** over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Voltage	V <sub>CC</sub> = 4.5V, I <sub>I</sub> =	-18 mA			-1.5	V
VOH	High Level Output Voltage	$I_{OH} = -0.4$ mA		V <sub>CC</sub> -2	HIO 6		٧
VOL	Voltage	V <sub>CC</sub> = 4.5V	54/74ALS I <sub>OL</sub> = 4 mA		0.25	0.4	V
			74ALS I <sub>OL</sub> = 8 mA		0.35	0.5	V
l <sub>l</sub>	Max High Input Current	$V_{CC} = 5.5V, V_{IH} = 7V$				0.1	mA
ΊΗ	High Level Input Current	$V_{CC} = 5.5V, V_{IH}$	= 2.7V	Ente		20	μΑ
IJĽ	Low Level Input Current	$V_{CC} = 5.5V, V_{IL}$	= 0.4V			-0.2	mA
IO	Output Drive Current	$V_{CC} = 5.5V$	V <sub>O</sub> = 2.25V	-30		-110	mA
ICC	Supply Current	$V_{CC} = 5.5V$	Outputs High		0.67	1.2	mA
		Outputs Low			1.10	2.0	mA

## Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter		DM54ALS21						
	Conditions	Min	Тур	Max	Min	Тур	Max	Unit
TPLH, Propagation delay time. Low to high level output	$V_{CC} = 4.5 \text{ to } 5.5V$ $R_L = 500 \Omega$ , $C_L = 50 \text{ pF}$ .	5	8	20	5	8	18	ns
TPHL, Propagation delay time. High to low level output		3	6	11	3	6	10	ns

## DM54ALS22/DM74ALS22 Dual 4-Input NAND Gates with Open Collector Outputs

#### **Features**

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

## **Absolute Maximum Ratings**

Supply Voltage	7V
Input Voltage	7V
Off State (High Level)	
Output Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	-55°C to 125°C

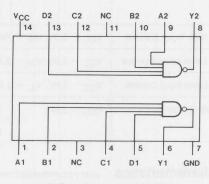
DM74ALS —55°C to 125°C

DM74ALS 0°C to 70°C

Storage Temperature Range —65°C to 150°C

## **Connection Diagram**

 $Y = \overline{ABCD}$ 



54ALS22 (J) 74ALS22 (J,N)

		DM54ALS2	2	1			
Parameter	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, VIH	2	Total L	0 10	2	O no		V
Low Level Input Voltage, VIL			0.8			0.8	V
High Level Output Voltage, VOH	HATEL BY SE		5.5			5.5	V
Low Level Output Current, IOL	rura rulipir -		4			8	mA

## Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Voltage	V <sub>CC</sub> = 4.5V, I <sub>I</sub> =	-18 mA	TOTAL PROPERTY.		-1.5	V
ЮН	High Level Output Current	$V_{CC} = 4.5V, V_{OH}$	H = 5.5V			100	μΑ
VOL	Low Level Output Voltage	V <sub>CC</sub> = 4.5V	54/74ALS I <sub>OL</sub> = 4 mA	Hatsiy	0.25	0.4	V
	ev ea es		74ALS I <sub>OL</sub> = 8 mA		0.35	0.5	V
II	Max High Input Current	V <sub>CC</sub> = 5.5V, V <sub>IH</sub>	= 7V			0.1	mA
ΙΗ	High Level Input Current	$V_{CC} = 5.5V, V_{IH}$	= 2.7V			20	μΑ
IIL	Low Level Input Current	$V_{CC} = 5.5V, V_{IL}$	$V_{CC} = 5.5V, V_{IL} = 0.4V$		e w	-0.2	mA
ICC	Supply Current	$V_{CC} = 5.5V$	Outputs High		0.22	0.4	mA
			Outputs Low		0.80	1.5	mA

## Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter		DM54ALS22			DM74ALS22			
	Conditions	Min	Тур	Max	Min	Тур	Max	Unit
TPLH, Propagation delay time. Low to high level output	$V_{CC}=4.5$ to 5.5V $R_L=2K~\Omega,$ $C_L=50~pF.$	23	27	59	23	27	54	ns
TPHL, Propagation delay time. High to low level output		8	11	32	8	11	26	ns

7V

## DM54ALS27/DM74ALS27 Triple 3-Input NOR Gates

#### **Features**

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

## **Absolute Maximum Ratings**

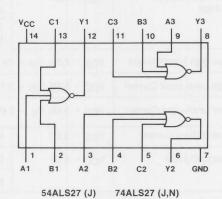
Supply Voltage Input Voltage Operating Free Air Temperature Range DM54ALS DM74ALS

Storage Temperature Range

7V -55°C to 125°C 0°C to 70°C -65°C to 150°C

## **Connection Diagram**

 $Y = \overline{A+B+C}$ 



	1	DM54ALS2	27	DM74ALS27			
Parameter	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, VIH	2			2	Y		V
Low Level Input Voltage, VIL	nul pec A		0.8			0.8	V
High Level Output Current, IOH	May Mejya.		-0.4			-0.4	mA
Low Level Output Current, IOL			4			8	mA

## Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Voltage	V <sub>CC</sub> = 4.5V, I <sub>I</sub> =	−18 mA			-1.5	V
Vон	High Level Output Voltage	$I_{OH} = -0.4$ mA		V <sub>CC</sub> -2			V
VOL	Voltage	V <sub>CC</sub> = 4.5V	54/74ALS I <sub>OL</sub> = 4 mA		0.25	0.4	V
			74ALS I <sub>OL</sub> = 8 mA		0.35	0.5	V
I <sub>I</sub>	Max High Input Current	$V_{CC} = 5.5V, V_{IH}$	$V_{CC} = 5.5V, V_{IH} = 7V$			0.1	mA
ΊΗ	High Level Input Current	$V_{CC} = 5.5V, V_{IH}$	= 2.7V			20	μΑ
IIL	Low Level Input Current	$V_{CC} = 5.5V, V_{IL}$	= 0.4V	Ownia A		-0.2	mA
IO	Output Drive Current	V <sub>CC</sub> = 5.5V	V <sub>O</sub> = 2.25V	-30		-110	mA
Icc	Supply Current	$V_{CC} = 5.5V$	Outputs High		0.97	1.8	mA
		Outputs Low			2.0	4.0	mA

## Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54ALS27						
		Min	Тур	Max	Min	Тур	Max	Unit
TPLH, Propagation delay time. Low to high level output	$V_{CC} = 4.5 \text{ to } 5.5 \text{V}$ $R_L = 500 \Omega$ , $C_L = 50 \text{pF}$ .	2	8	15	2	8	13	ns
TPHL, Propagation delay time. High to low level output		2	3	10	2	3	9	ns

## DM54ALS28/DM74ALS28 Quadruple 2-Input NOR Buffers

#### **Features**

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with LS TTL Counterpart.
- Improved AC Performance Over LS28.
- Improved Line Receiving Characteristics.

#### **Absolute Maximum Ratings**

Supply Voltage Input Voltage Operating Free Air Temperature Range

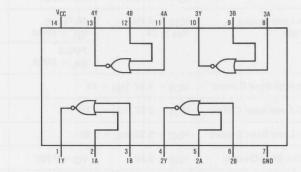
DM54ALS28 DM74ALS28

Storage Temperature Range

7V -55°C to 125°C

0°C to 70°C -65°C to 150°C

### **Connection Diagram**



74ALS28 (J,N)

54ALS28 (J)

 $Y = \overline{A + B}$ 

Parameter		OM54ALS2	28	1			
	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, VCC	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, VIH	2			2			٧
Low Level Input Voltage, VIL			0.8			0.8	V
High Level Output Current, IOH		The last	-1.0			-2.6	mA
Low Level Output Current, IOL	3-1-1	fydlefd	12	peal and	e protest	24	mA

## Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Nom	Max	Unit
VIK	Input Clamp Voltage	$V_{CC} = 4.5V, I_{I} = -$	−18 mA			-1.5	V
Vон	High Level Output Voltage	$V_{CC} = 4.5V$ $V_{IL} = V_{IL} MAX$	54/74ALS I <sub>OH</sub> = -1mA	2.4	3.2	witter	V
		74ALS I <sub>OH</sub> = -2.6mA	2.4	3.3		V	
		$I_{OH} = -400\mu A$	54/74ALS	V <sub>CC</sub> -2			V
VOL	Low Level Output Voltage	$V_{CC} = 4.5V$ $V_{IH} = 2V$	54/74ALS I <sub>OL</sub> = 12mA		0.25	0.4	٧
			74ALS I <sub>OL</sub> = 24mA		0.35	0.5	V
l <sub>I</sub>	Max High Input Current	V <sub>CC</sub> = 5.5V, V <sub>IH</sub> =	= 7V			0.1	mA
IIH	High Level Input Current	V <sub>CC</sub> = 5.5V, V <sub>IH</sub> =	= 2.7V			20	μΑ
IIL	Low Level Input Current	V <sub>CC</sub> = 5.5V, V <sub>IL</sub> =	= 0.4V			-0.2	mA
10	Output Drive Current	$V_{CC} = 5.5V$	$V_{O} = 2.25V$	-30		-110	mA
Іссн	Supply Current	Outputs High V <sub>CC</sub> = 5.5V, VI = 0V			1.7	2.8	mA
ICCL	Supply Current	Outputs Low $V_{CC} = 5.5V$ , $VI = 4.5V$			4.8	8.0	mA

## Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54ALS28						
		Min	Тур	Max	Min	Тур	Max	Unit
TPLH, Propagation delay time. Low to high level output	$V_{CC} = 4.5 \text{ to } 5.5V$ $R_L = 500  \Omega,$ $C_L = 50  pF.$	2		10	2		8	ns
TPHL, Propagation delay time. High to low level output		3		10	3		8	ns

## DM54ALS30/DM74ALS30 8 Input NAND Gate

#### **Features**

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

## **Absolute Maximum Ratings**

Supply Voltage Input Voltage Operating Free Air Temperature Range DM54ALS

DM74ALS DM74ALS

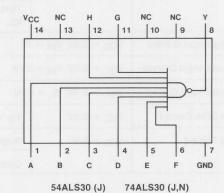
Storage Temperature Range

7V 7V

-55°C to 125°C 0°C to 70°C -65°C to 150°C

## **Connection Diagram**

Y = ABCDEFGH



1

	DM54ALS30			1			
Parameter	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, V <sub>CC</sub>	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, VIH	2			2			V
Low Level Input Voltage, VIL			0.8			0.8	V
High Level Output Current, IOH		1009	-0.4	property by		-0.4	m.A
Low Level Output Current, IOL		1 valigue	4	Smill but	Hat is	8	mA

## Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Voltage	V <sub>CC</sub> = 4.5V, I <sub>I</sub> =	-18 mA			-1.5	V
VOH	High Level Output Voltage	$I_{OH} = -0.4$ mA		V <sub>CC</sub> -2	old in		V
VOL	Low Level Output Voltage	V <sub>CC</sub> = 4.5V	54/74ALS I <sub>OL</sub> = 4 mA		0.25	0.4	٧
		a la di	74ALS I <sub>OL</sub> = 8 mA		0.35	0.5	V
II.	Max High Input Current	$V_{CC} = 5.5V, V_{IH} = 7V$				0.1	mA
Ιн	High Level Input Current	$V_{CC} = 5.5V, V_{IH}$	= 2.7V			20	μΑ
IIL	Low Level Input Current	$V_{CC} = 5.5V, V_{IL}$	= 0.4V	HISTORISE		-0.4	mA
IO	Output Drive Current	$V_{CC} = 5.5V$	$V_0 = 2.25V$	-30		-110	mA
ICC	Supply Current	$V_{CC} = 5.5V$	Outputs High		0.22	0.36	mA
			Outputs Low		0.54	0.90	mA

## Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54ALS30						
		Min	Тур	Max	Min	Тур	Max	Unit
TPLH, Propagation delay time. Low to high level output	$V_{CC} = 4.5 \text{ to } 5.5V$ $R_L = 500 \Omega,$ $C_L = 50 \text{pF}.$	2	4	10	2	4	9	ns
TPHL, Propagation delay time. High to low level output		5	9	17	5	9	15	ns

## DM54ALS32/DM74ALS32 Quad 2-Input OR Gates

#### **Features**

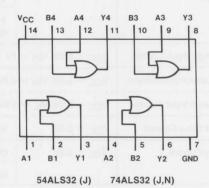
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

## **Absolute Maximum Ratings**

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	-55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	-65°C to 150°C

## **Connection Diagram**

Y = A + B



	1	DM54ALS3	12	DM74ALS32			11-14
Parameter	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, VIH	2			2			V
Low Level Input Voltage, VIL			0.8			0.8	٧
High Level Output Current, IOH	atto v isam	tuid	-0.4	mad pr		-0.4	mA
Low Level Output Current, IOL		Time	4	Auto Just		8	mA

## **Electrical Characteristics** over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Voltage	V <sub>CC</sub> = 4.5V, I <sub>I</sub> =	-18 mA			-1.5	V
VOH	High Level Output Voltage	$I_{OH} = -0.4$ mA		V <sub>CC</sub> -2	部队件	## (F) (C)	٧
VOL	Low Level Output Voltage	V <sub>CC</sub> = 4.5V	54/74ALS I <sub>OL</sub> = 4 mA		0.25	0.4	V
	1 2 2		1 TALES		0.35	0.5	٧
IĮ	Max High Input Current	$V_{CC} = 5.5V, V_{IH}$	= 7V			0.1	mA
ΙΗ	High Level Input Current	$V_{CC} = 5.5V, V_{IH}$	= 2.7V	Mar A	= 7	20	μΑ
IIL	Low Level Input Current	$V_{CC} = 5.5V, V_{IL}$	= 0.4V			-0.2	mA
IO	Output Drive Current	$V_{CC} = 5.5V$	V <sub>O</sub> = 2.25V	-30		-110	mA
Icc	Supply Current	$V_{CC} = 5.5V$	Outputs High		1.9	4.0	mA
	and the same	e lavember	Outputs Low		2.6	4.9	mA

## Switching Characteristics over recommended operating free air temperature range (Note 1)

		DM54ALS32			DM74ALS32			
Parameter	Conditions	Min	Тур	Max	Min	Тур	Max	Unit
TPLH, Propagation delay time. Low to high level output	$V_{CC} = 4.5 \text{ to } 5.5V$ $R_L = 500 \Omega,$ $C_L = 50 \text{pF}.$	3	6	13	3	6	12	ns
TPHL, Propagation delay time. High to low level output		2	5	12	2	5	11	ns

## DM54ALS33/DM74ALS33 Quadruple 2-Input NOR Buffers with Open-Collector Outputs

#### **Features**

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced, Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with LS TTL Counterpart.
- Improved AC Performance Over LS33.
- Improved Line Receiving Characteristics.

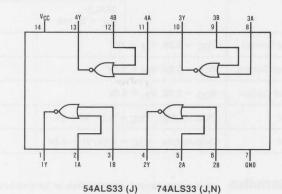
#### **Absolute Maximum Ratings**

Supply Voltage

Input Voltage

Off State (High Level)	
Output Voltage	7V
Operating Free Air Temperature Range	
DM54ALS33	-55°C to 125°C
DM74ALS33	0°C to 70°C
Storage Temperature Range	-65°C to 150°C

### **Connection Diagram**



 $Y = \overline{A + B}$ 

	DM54ALS33						
Parameter	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, V <sub>CC</sub>	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, VIH	2			2			V
Low Level Input Voltage, VIL	ntrast t		0.8			0.8	V
High Level Output Voltage, VOH	day dept de		5.5	Opin pa	az literii.	5.5	V
Low Level Output Current, IOL	ar as as a second		12	miles by a legitura		24	mA

## **Electrical Characteristics** over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Тур	Max	Unit	
VIK	Input Clamp Voltage	V <sub>CC</sub> = 4.5V, I <sub>I</sub> =	-18 mA			-1.5	V	
ЮН	High Level Output Current	V <sub>CC</sub> = 4.5V, V <sub>OH</sub>	y = 5.5V			100	μΑ	
VOL	VOL Low Level Output Voltage			54/74ALS I <sub>OL</sub> = 12 mA		0.25	0.4	V
			74ALS I <sub>OL</sub> = 24 mA		0.35	0.5	V	
l <sub>I</sub>	Max High Input Current	$V_{CC} = 5.5V, V_{IH}$	= 7V			0.1	mA	
IIH	High Level Input Current	$V_{CC} = 5.5V, V_{IH}$	= 2.7V			20	μΑ	
IIL	Low Level Input Current	$V_{CC} = 5.5V, V_{IL}$	= 0.4V			-0.2	mA	
ІССН	Supply Current	Outputs High $V_{CC} = 5.5V$ , $VI = 0V$			1.7	2.8	mA	
ICCL	Supply Current	Outputs Low Vo	C = 5.5V, VI = 4.5V		4.8	8.	mA	

## Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter		DM54ALS33						
	Conditions	Min	Тур	Max	Min	Тур	Max	Unit
TPLH, Propagation delay time. Low to high level output	$V_{CC} = 4.5V \text{ to } 5.5V$ $R_{L} = 667 \Omega$ $C_{L} = 50 \text{ pF}$	10		40	10		30	ns
TPHL, Propagation delay time. High to low level output		7		18	7		15	ns

## DM54ALS37/DM74ALS37 Quadruple 2-Input NAND Buffers

#### **Features**

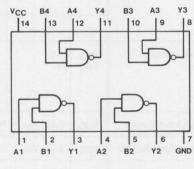
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced, Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with LS TTL Counterpart.
- Improved AC Performance Over LS37.
- Improved Line Receiving Characteristics.

#### **Absolute Maximum Ratings**

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS37	-55°C to 125°C
DM74ALS37	0°C to 70°C
Storage Temperature Range	-65°C to 150°C

## **Connection Diagram**

 $Y = \overline{AB}$ 



	1	DM54ALS37			DM74ALS37			
Parameter	Min	Nom	Max	Min	Nom	Max	Unit	
Supply Voltage, VCC	4.5	5	5.5	4.5	5	5.5	V	
High Level Input Voltage, VIH	2			2			V	
Low Level Input Voltage, VIL			0.8			0.8	V	
High Level Output Current, IOH			-1.0			-2.6	mA	
Low Level Output Current, IOL		v-maint	12			24	mA	

## Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Voltage	V <sub>CC</sub> = 4.5V, I <sub>I</sub> =	-18 mA			-1.5	V
Vон	High Level Output Voltage	V <sub>CC</sub> = 4.5V V <sub>IL</sub> = V <sub>IL</sub> MAX	54/74ALS I <sub>OH</sub> = -1mA	2.4	3.2	1111	V
	- 12 FL NO		74ALS I <sub>OH</sub> = -2.6mA	2.4	3.3		V
		$I_{OH} = -400\mu A$	54/74ALS	V <sub>CC</sub> -2			٧
VOL Low Level Output Voltage	V <sub>CC</sub> = 4.5V V <sub>IH</sub> = 2V	54/74ALS I <sub>OL</sub> = 12mA		0.25	0.4	V	
	Voltage V <sub>IH</sub> = 2V	i rab	74ALS I <sub>OL</sub> = 24mA	84.	0.35	0.5	٧
l <sub>l</sub>	Max High Input Current	$V_{CC} = 5.5V, V_{IH} =$	= 7V			0.1	mA
lін	High Level Input Current	$V_{CC} = 5.5V, V_{IH} =$	= 2.7V			20	μΑ
IIL	Low Level Input Current	V <sub>CC</sub> = 5.5V, V <sub>IL</sub> =	= 0.4V			-0.2	mA
IO	Output Drive Current	$V_{CC} = 5.5V$	$V_{O} = 2.25V$	-30		-110	mA
Іссн	Supply Current	Outputs High VCC	S = 5.5V, VI = 0V		0.86	1.6	mA
ICCL	Supply Current	Outputs Low VCC	; = 5.5V, VI = 4.5V		4.0	6.4	mA

## Switching Characteristics over recommended operating free air temperature range (Note 1)

		DM54ALS37						
Parameter	Conditions	Min	Тур	Max	Min	Тур	Max	Unit
T <sub>PLH</sub> , Propagation delay time. Low to high level output	$V_{CC} = 4.5 \text{ to } 5.5V$ $R_{L} = 500 \Omega$ $C_{L} = 50 \text{ pF}$	2		10	2		8	ns
TPHL, Propagation delay time. High to low level output		3		10	3		8	ns

## DM54ALS38/DM74ALS38 Quadruple 2-Input NAND Buffers with Open-Collector Outputs

#### **Features**

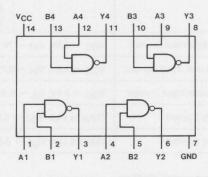
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with LS TTL Counterpart.
- Improved AC Performance Over LS38.
- Improved Line Receiving Characteristics.

#### **Absolute Maximum Ratings**

Supply Voltage	/V
Input Voltage	7V
Off State (High Level)	
Output Voltage	7V
Operating Free Air Temperature Range	
DM54ALS38	-55°C to 125°C
DM74ALS38	0°C to 70°C
Storage Temperature Range	-65°C to 150°C

#### **Connection Diagram**

 $Y = \overline{AB}$ 



	1	M54ALS3	18				
Parameter	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, VCC	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, VIH	2	egin.	Table	2	Hille		V
Low Level Input Voltage, VIL			0.8			0.8	V
High Level Output Voltage, VOH			5.5			5.5	V
Low Level Output Current, IOL			12	swill in		24	mA

## Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Voltage	V <sub>CC</sub> = 4.5V, I <sub>I</sub> =	-18 mA			-1.5	V
ЮН	High Level Output Current	VCC = 4.5V, V <sub>OF</sub>	H = 5.5V			100	μΑ
VOL	Low Level Output Voltage	V <sub>CC</sub> = 4.5V V <sub>IH</sub> = 2V	54/74ALS I <sub>OL</sub> = 12mA		0.25	0.4	V
	27 24 25 1		74ALS IOL = 24mA		0.35	0.5	٧
lį	Max High Input Current	V <sub>CC</sub> = 5.5V, V <sub>IH</sub>	= 7V			0.1	mA
ΊΗ	High Level Input Current	V <sub>CC</sub> = 5.5V, V <sub>IH</sub>	= 2.7V			20	μΑ
IIL	Low Level Input Current	$V_{CC} = 5.5V, V_{IL}$	= 0.4V			-0.2	mA
ІССН	Supply Current	Outputs High $V_{CC} = 5.5V$ , $VI = 0V$			0.86	1.6	mA
ICCL	Supply Current	Outputs Low VCC	c = 5.5V, VI = 4.5V		4.0	6.4	mA

## Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter		DM54ALS38			DM74ALS38			
	Conditions	Min	Тур	Max	Min	Тур	Max	Unit
TPLH, Propagation delay time. Low to high level output	$V_{CC} = 4.5 \text{ to } 5.5V$ $R_L = 667 \Omega$ , $C_L = 50 \text{ pF}$	10		40	10		30	ns
TPHL, Propagation delay time. High to low level output		7		18	7		15	ns



## DM54ALS40/DM74ALS40 Dual 4-Input NAND Buffers

#### **Features**

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with LS TTL Counterpart.
- Improved AC Performance Over LS40.
- Improved Line Receiving Characteristics.

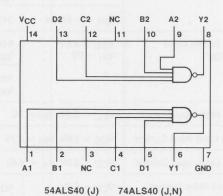
#### **Absolute Maximum Ratings**

Supply Voltage
Input Voltage
Operating Free Air Temperature Range
DM54ALS40
DM74ALS40

Storage Temperature Range

-55°C to 125°C 0°C to 70°C -65°C to 150°C

## **Connection Diagram**



 $Y = \overline{ABCD}$ 

	1	DM54ALS4	10				
Parameter	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, VCC	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, VIH	2			2			V
Low Level Input Voltage, VIL			0.8	10 TO 2015		0.8	V
High Level Output Current, IOH	Militeral - 1	To the	-1.0			-2.6	mA
Low Level Output Current, IOL		plicate	12	est bein	Minney B	24	mA

## Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Voltage	$V_{CC} = 4.5V, I_{I} = -$	-18 mA			-1.5	V
VOH	High Level Output Voltage	V <sub>CC</sub> = 4.5V V <sub>IL</sub> = V <sub>IL</sub> MAX	54/74ALS I <sub>OH</sub> = -1mA	2.4	3.2	- (Datata	V
			74ALS I <sub>OH</sub> = -2.6mA	2.4	3.3		V
	0.00	$I_{OH} = -400\mu A$	54/74ALS	V <sub>CC</sub> -2			٧
VOL	Low Level Output Voltage	V <sub>CC</sub> = 4.5V V <sub>IH</sub> = 2V	54/74ALS I <sub>OL</sub> = 12mA		0.25	0.4	V
			74ALS I <sub>OL</sub> = 24mA		0.35	0.5	V
l <sub>l</sub>	Max High Input Current	V <sub>CC</sub> = 5.5V, V <sub>IH</sub> =	= 7V	300a - r		0.1	mA
IH	High Level Input Current	V <sub>CC</sub> = 5.5V, V <sub>IH</sub> =	= 2.7V			20	μΑ
IIL	Low Level Input Current	V <sub>CC</sub> = 5.5V, V <sub>IL</sub> =	= 0.4V			-0.2	mA
IO	Output Drive Current	$V_{CC} = 5.5V$	$V_{O} = 2.25V$	-30		-110	mA
ICCH	Supply Current	Outputs High VCC	$_{\rm C} = 5.5 \text{V},  \text{VI} = 0 \text{V}$		0.43	0.8	mA
ICCL	Supply Current	Outputs Low VCC	; = 5.5V, VI = 4.5V		2.0	3.2	mA

## Switching Characteristics over recommended operating free air temperature range (Note 1)

		DM54ALS40						
Parameter	Conditions	Min	Тур	Max	Min	Тур	Max	Unit
TPLH, Propagation delay time. Low to high level output	$V_{CC} = 4.5 \text{ to } 5.5V$ $R_L = 500 \Omega$ , $C_L = 50 \text{ pF}$ .	2		10	2		8	ns
TPHL, Propagation delay time. High to low level output		3		10	3		8	ns



## DM54ALS74/DM74ALS74 Dual D Positive-Edge-Triggered Flip-Flops with Preset and Clear

#### **General Description**

The DM54ALS74 is a dual edge-triggered flip-flops. Each flip-flop has individual D, clock, clear and preset inputs, and also complementary Q and  $\bar{Q}$  outputs.

Information at input D is transferred to the Q output on the positive going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. When the clock input is at either the high or low level, the D input signal has no effect.

Asynchronous preset and clear inputs will set or clear Q output respectively upon the application of low level signal.

#### **Features**

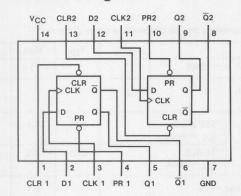
Switching Specifications at 50 pF.

- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process
- Functionally and Pin-For-Pin Compatible with Schottky and LS TTL Counterpart.
- Improved AC Performance Over LS74 at Approximately Half the Power.

#### **Absolute Maximum Ratings**

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	-55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	-65°C to 150°C

#### **Connection Diagram**



54ALS74 (J) 74ALS74 (J,N)

#### **Function Table**

	Inp	uts		Out	puts
PR	CLR	CLK	D	Q	Q
L	Н	X	X	Н	L
Н	L	X	X	L	Н
L	L	X	X	H*	H*
Н	Н	1	Н	H	L
Н	Н	1	L	L	Н
Н	Н	L	X	Q <sub>0</sub>	Q <sub>0</sub>

- L = Low State, H = High State, X = Don't Care
- $\uparrow =$  Positive Edge Transition
- $Q_0 = Previous Condition of Q$
- \*= This condition is nonstable; it will not persist when preset and clear inputs return to their inactive (high) level. The output levels in this condition are not guaranteed to meet the V<sub>OH</sub> specification.

			M54ALS7	4		M74ALS7	4	
Parameter		Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, V <sub>CC</sub>	i-sylling in	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, VIH	rebiO beat	2			2			V
Low Level Input Voltage, VIL				0.8			0.8	V
High Level Output Current, IOH	h Level Output Current, IOH		Taratt de chi	-0.4		- E (18 3	-0.4	mA
Low Level Output Current, IOL				4	obuezuki Luar (J. Bers		8	mA
Clock frequency, fCLOCK		0		30	0		34	МН
Width of Clock Pulse, Tw	High	14		es pase	12		Harri I	ns
	Low	19	A LOUIS DE	Samuel a	17	Li Lierini		ns
Pulse Width T <sub>W</sub> , Preset & Clear	Low	15			15			ns
Data Setup Time, T <sub>SU</sub>	Data	15↑			15↑			ns
Data Setup Time, TSU	PRE or CLR Inactive	10↑			10↑	mala		ns
Data Hold Time, TH		0↑			0↑			ns

The (†) arrow indicates the positive edge of the Clock is used for reference.

## Electrical Characteristics over recommended operating free air temperature range (Note 1)

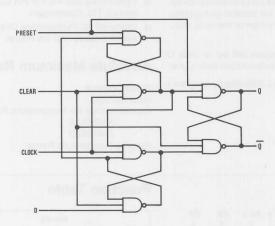
	Parameter		Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Vol	tage	$V_{CC} = 4.5V$ II	= -18mA			-1.5	V
VOH	High Level Outp Voltage	out	$I_{OH} = -400\mu A$		V <sub>CC</sub> -2			V
VOL	OL Low Level Output Voltage		V <sub>CC</sub> = 4.5V V <sub>IH</sub> = 2V	54/74ALS I <sub>OL</sub> = 4mA		0.25	0.4	V
				0.5	V			
lį	Max High Input	Current	V <sub>CC</sub> = 5.5V V <sub>IH</sub> = 7V			A TX	0.1	mA
I <sub>IH</sub>	High Level	Clock, D	$V_{CC} = 5.5V  V_{IH} = 2.7V$			MTR-THE	20	μΑ
	Input Current	Preset, Clear					40	μΑ
IIL	Low Level	Clock, D	$V_{CC} = 5.5V V$	IL = 0.4V			-0.2	mA
	Input Current	Preset, Clear					-0.4	mA
10	Output Drive Cu	irrent	$V_{CC} = 5.5V V$	O = 2.25V	-30		-110	mA
Icc	Supply Current		$V_{CC} = 5.5V$			2.4	4	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter		То		D	M54ALS	74	DM74ALS74			
	From		Conditions	Min	Тур	Max	Min	Тур	Max	Unit
FMAX			diam'r 10 to 10	30	0.00		34		0.18	MHz
TPLH	Preset	Q	V <sub>CC</sub> = 4.5V to 5.5V	2	5	11	2	5	10	ns
TPHL	or clear	u u		4	8	15	4	8	13	ns
T <sub>PLH</sub>	Clock	Q	$R_L = 500 \Omega$ $C_L = 50 pF$	4	7	16	4	7	14	ns
TPHL	Name of the last o	Na da hi	S. D. W. WHICH SHOW AND ADDRESS OF	5	10	20	5	10	17	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-3.

## **Logic Diagram**



National Semiconductor

Preliminary

## DM54ALS109/DM74ALS109 Dual J-K Positive-Edge-Triggered Flip-Flops with Preset and Clear

## **General Description**

The DM54ALS109 is a dual edge-triggered flip flops. Each flip flop has individual J,  $\bar{K}$ , clock, clear and preset inputs, and also complementary Q and  $\bar{Q}$  outputs.

Information at input J or  $\bar{K}$  is transferred to the Q output on the positive going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. When the clock input is at either the high or low level, the J,  $\bar{K}$  input signal has no effect.

Asynchronous preset and clear inputs will set or clear Q output respectively upon the application of low level signal.

The  $J \, \overline{K}$  design allows operation as a D flip flop by tying the J and  $\overline{K}$  inputs together.

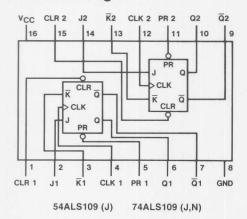
#### **Features**

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and LS TTL Counterpart.
- Improved AC Performance Over LS109 at Approximately Half the Power.

#### **Absolute Maximum Ratings**

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	-55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	-65°C to 150°C

#### **Connection Diagram**



#### **Function Table**

		Inputs			Out	puts
PR	CLR	CK	J	K	Q	Q
L	Н	X	X	X	Н	L
Н	L	X	X	X	L	Н
L	L	X	X	X	H*	H*
Н	Н	1	L	L	L	Н
Н	Н	1	Н	L	TOG	GLE
Н	Н	1	L	Н	Q <sub>0</sub>	$\overline{Q}_0$
Н	Н	1	Н	Н	H	L
Н	Н	L	X	X	Q <sub>0</sub>	$\overline{Q}_0$

L = Low State, H = High State, X = Don't Care

 $1 = Positive Edge Transition, Q_0 = Previous Condition of Q$ 

 $<sup>^{\</sup>circ}$  This condition is nonstable; it will not persist when present and clear inputs return to their inactive (high) level. The output levels in this condition are not guaranteed to meet the V<sub>OH</sub> specification.

		D	M54ALS1	09	D	M74ALS1	09	
Parameter		Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, V <sub>CC</sub>	61 BE	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, VIH		2	HI Irek	154	2			V
Low Level Input Voltage, VIL				0.8			0.8	V
High Level Output Current	, Іон			-0.4			-0.4	mA
Low Level Output Current,	loL			4			8	mA
Clock Frequency, fCLOCK		0		30	0		34	MH
Pulse Width Tw	Clock High	14			12	No.	music	ns
r dise viralii i yy	Clock Low	19			17			ns
Pulse Width T <sub>W</sub> , Preset &	Clear	15	-40		15			ns
Data Setup Time, TSU	J or K	15↑			15↑			ns
Data Setup Time, 150	PRE or CLR inactive	10↑			101			
Data Hold Time, TH		01			0↑			ns

The (†) arrow indicates the positive edge of the Clock is used for reference.

## Electrical Characteristics over recommended operating free air temperature range (Note 1)

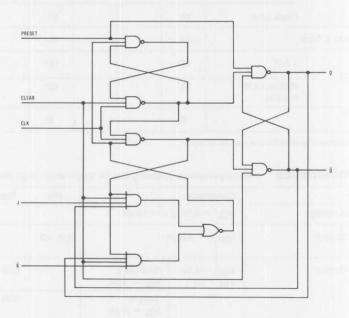
	Parameter		Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Vol	tage	$V_{CC} = 4.5V I_I$	=-18mA			-1.5	V
Vон	High Level Outp Voltage	ut	$I_{OH} = -400\mu A$		V <sub>CC</sub> -2			V
VOL	Low Level Outp Voltage	ut	$V_{CC} = 4.5V$ $V_{IH} = 2V$	54/74ALS I <sub>OL</sub> = 4mA		0.25	0.4	V
				74ALS I <sub>OL</sub> = 8mA		0.35	0.5	V
lı .	Max High Input	Current	$V_{CC} = 5.5V V_{IH} = 7V$				0.1	mA
Ін	High Level	Clock, J, K	$V_{CC} = 5.5 V V_{IH} = 2.7 V$				20	μΑ
	Input Current	Preset, Clear					40	
IIL	Low Level	Clock, J, K	$V_{CC} = 5.5 V V$	IL = 0.4V			-0.2	mA
	Input Current	Preset, Clear					-0.4	
10	Output Drive Current	$V_{CC} = 5.5V$	$V_0 = 2.25V$	V <sub>O</sub> = 2.25V			-110	mA
Icc	Supply Current		$V_{CC} = 5.5V$			2.4	4	mA

## Switching Characteristics over recommended operating free air temperature range (Note 1)

	ggrat_Labrin	То	Conditions	DI	DM54ALS109			DM74ALS109		
Parameter	From			Min	Тур	Max	Min	Тур	Max	Unit
FMAX		100	1 88 1 6 1	30	50		34	50	Herry	MHz
TPLH	Preset	Q	$V_{CC} = 4.5V \text{ to } 5.5V$	2	5	11	2	5	10	ns
T <sub>PHL</sub>	or clear		$R_L = 500 \Omega$ $C_L = 50 pF$	4	8	15	4	8	13	ns
T <sub>PLH</sub>	011			4	7	16	4	7	14	ns
TPHL	Clock Q			5	10	20	5	10	17	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-3.

## **Logic Diagram**



## DM54ALS131/DM74ALS131 3-Line to 8-Line Decoder/Demultiplexer with Address Register

#### **General Description**

The ALS131 is a three-line to eight-line decoder/demultiplexer with registers on the three address inputs. When the clock transitions from low to high, the address present at the select inputs (A, B, and C) is stored in the latches. The output enable controls, G1 and G2, control the state of the outputs independently of the select or clock inputs. All of the outputs are high unless G1 is high and  $\bar{\mathbb{G}}2$  is low. The ALS131 is ideally suited for implementing glitch-free decoders in strobed (stored-address) applications in bus-oriented systems.

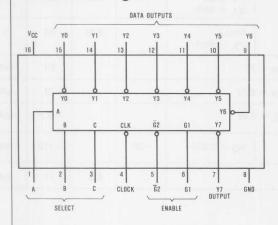
#### **Features**

- Combines Decoder and 3-Bit Address Register.
- Incorporates 3 Enable Inputs to Simplify Cascading.
- Low Power Dissipation . . . 28mW Typ
- Switching Specification Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.

### **Absolute Maximum Ratings**

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Rang	je
DM54ALS131	-55°C to 125°C
DM74ALS131	0°C to 70°C
Storage Temperature Range	-65°C to 150°C

## **Connection Diagram**



54ALS131 (J) 74ALS131 (J,N)

#### **Function Table**

Inputs									Out	puts			
			S	elec	ct				Out	put			
CLK	G1	G2	С	В	Α	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Υ7
X	X	Н	X	X	X	Н	Н	Н	Н	Н	Н	Н	Н
X	L	Χ	X	X	Χ	Н	Н	Н	Н	Н	Н	Н	Н
1	Н	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н
1	Н	L	L	L	Н	Н	L	Н	Н	Н	Н	Н	Н
1	Н	L	Н	Н	L	Н	Н	L	Н	Н	Н	Н	Н
1	Н	L	L	Н	Н	Н	Н	Н	L	Н	Н	Н	Н
1	Н	L	Н	L	L	Н	Н	Н	Н	L	Н	Н	Н
1	Н	L	Н	L	Н	Н	Н	Н	Н	Н	L	Н	Н
1	Н	L	Н	L	Н	Н	Н	Н	Н	Н	L	Н	Н
1	Н	L	Н	Н	L	Н	Н	Н	Н	Н	Н	L	Н
L	Н	L	X	X	X	Output corresponding to stored address, L; all others, H.							

H = High Level, L = Low Level, X = Don't Care

T = Transition from Low to High Level

Parameter			D					
		Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, V <sub>CC</sub>		4.5	5	5.5	4.5	5	5.5	٧
High Level Input Voltage, VIH		2			2	<b>-6</b> o		V
Low Level Input Voltage, VIL				0.8		nen)	0.8	٧
High Level Output Current, IOH				-0.4			-0.4	mA
Low Level Output Current, IOL				4			8	mA
Clock Frequency, FCLOCK		0		40	0		50	MHz
Width of Clock Pulse, TW		15			10	a Alama		ns
Setup Time, TSU	A, B, C	151			10↑			ns
Hold Time, T <sub>H</sub>	A, B, C	01			01			ns

## **Electrical Characteristics** over recommended operating free air temperature range (Note 1)

Parameter		Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Voltage	V <sub>CC</sub> = 4.5V, I <sub>I</sub> =			-1.5	V	
Vон	High Level Output Voltage	$I_{OH} = -0.4$ mA	V <sub>CC</sub> -2			V	
VOL Low Level Out	Low Level Output Voltage	V <sub>CC</sub> = 4.5V	54/74ALS I <sub>OL</sub> = 4mA	manga i ma en	0.25	0.4	V
	Estg/MO Footb		74ALS I <sub>OL</sub> = 8mA		0.35	0.5	V
lı —	Max High Input Current	V <sub>CC</sub> = 5.5V, V <sub>IH</sub>			0.1	mA	
ΊΗ	High Level Input Current	V <sub>CC</sub> = 5.5V, V <sub>IH</sub>			20	μΑ	
IĮL	Low Level Input Current	$V_{CC} = 5.5V, V_{IL}$			-0.2	mA	
10	Output Drive Current	V <sub>CC</sub> = 5.5V	V <sub>O</sub> = 2.25V	-30		-110	mA
Icc	Supply Current	VCC = 5.5V			5.5	11	mA

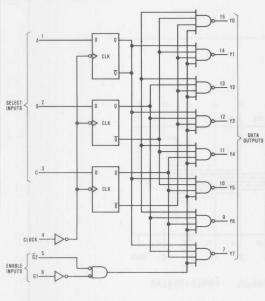
## 1

## Switching Characteristics over recommended operating free air temperature range (Note 1)

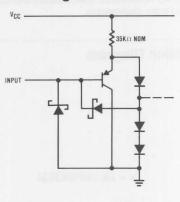
Parameter		Conditions	DI	M54ALS1	131	DI			
	From (Input)		Min	Тур	Max	Min	Тур	Max	Unit
T <sub>PLH</sub>	G2	G2	5	7	18	5	7	15	ns
TPHL	02		5	7.5	18	5	7.5	15	
TPLH	G1	$V_{CC} = 4.5 \text{ to } 5.5 \text{V}$	7	10	24	7	10	20	
TPHL	Clock	$R_{L} = 500 \Omega$ $C_{I} = 50 \text{ pF}$	6	10	20	6	10	17	
TPLH			8	10	26	8	10	23	
TPHL	and an analysis		7	10	24	7	10	20	ns

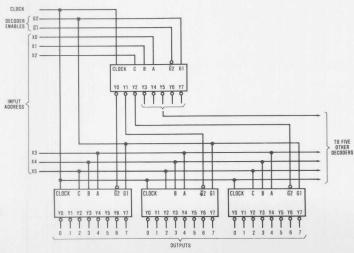
NOTE 1: See notes pg. 1-iii, figures pg. 3-3.

## **Logic Diagrams**



## **Schematic Diagram**





# DM54ALS133/DM74ALS133 13-Input NAND Gate

#### **Features**

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

### **Absolute Maximum Ratings**

Supply Voltage

Input Voltage
Operating Free Air Temperature Range

DM54ALS DM74ALS

-55°C to 125°C 0°C to 70°C -65°C to 150°C

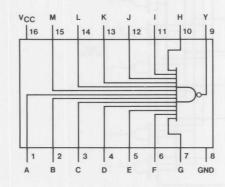
7V

7V

Storage Temperature Range

# **Connection Diagram**

Y = ABCDEFGHIJKLM



54ALS133 (J) 74ALS133 (J,N)

	D	M54ALS1	33	D	33		
Parameter	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, VIH	2		Manala	2			V
Low Level Input Voltage, VIL			0.8			0.8	V
High Level Output Current, IOH	d r ola koan		-0.4			-0.4	m.A
Low Level Output Current, IOL			4			8	mA

# Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions	Conditions		Тур	Max	Unit
VIK	Input Clamp Voltage	$V_{CC} = 4.5V$ , $I_{I} = -18mA$				-1.5	٧
Vон	High Level Output Voltage	$I_{OH} = -0.4$ mA	Made shall to the state of the	V <sub>CC</sub> -2			٧
VOL	Low Level Output Voltage	V <sub>CC</sub> = 4.5V	54/74ALS IOL = 4mA		0.25	0.4	V
			74 ALS I <sub>OL</sub> = 8mA		0.35	0.5	V
lį	Max High Input Current	$V_{CC} = 5.5V, V_{IH}$	= 7V			0.1	mA
Ін	High Level Input Current	$V_{CC} = 5.5V, V_{IH}$	= 2.7V		iteride	20	μΑ
l <sub>IL</sub>	Low Level Input Current	$V_{CC} = 5.5V, V_{IL}$	= 0.4V			-0.4	mA
lo	Output Drive Current	$V_{CC} = 5.5V$	$V_0 = 2.25V$	-30		-110	mA
Icc	Supply Current	$V_{CC} = 5.5V$	Outputs High		0.24	0.34	mA
			Outputs Low		0.56	0.80	m.A

# Switching Characteristics over recommended operating free air temperature range (Note 1)

		D	D	13 15				
Parameter	Conditions	Min	Тур	Max	Min	Тур	Max	Unit
TPLH, Propagation delay time. Low to high Level Output	$V_{CC} = 4.5 \text{ to } 5.5V$ $R_L = 500  \Omega$ , $C_L = 50  \text{pF}$ .	2	4	10	2	4	9	ns
TPHL, Propagation delay time. High to low Level Output		5	10	25	5	10	22	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-1.



# DM54ALS137/DM74ALS137 3-Line to 8-Line Decoder/Demultiplexer with Address Latches

#### **General Description**

The ALS137 is a three-line to eight-line decoder/demultiplexer with latches on the three address inputs. When the latch-enable input ( $\overline{GL}$ ) is low, the ALS137 acts as a decoder/demultiplexer. When  $\overline{GL}$  goes from low to high, the address present at the select inputs (A, B, and C) is stored in the latches. Further address changes are ignored as long as  $\overline{GL}$  remains high. The output enable controls, G1 and  $\overline{G2}$ , control the state of the outputs independently of the select or latch-enable inputs. All of the outputs are high unless G1 is high and  $\overline{G2}$  is low. The ALS137 is ideally suited for implementing glitch-free decoders in strobed (stored-address) applications in bus-oriented systems.

#### **Features**

Combines Decoder and 3-Bit Address Latch.

- Incorporates 3 Enable Inputs to Simplify Cascading.
- Low Power Dissipation . . . 28 mW Typ.
- Switching Specifications Guaranteed over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.

### **Absolute Maximum Ratings**

 Supply Voltage
 7V

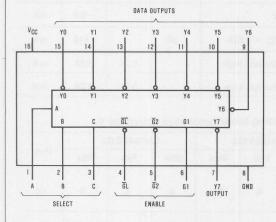
 Input Voltage
 7V

 Operating Free Air Temperature Range
 -55°C to 125°C

 DM54ALS137
 -0°C to 70°C

 Storage Temperature Range
 -65°C to 150°C

### **Connection Diagram**



54ALS137 (J) 74ALS137 (J,N)

#### **Function Table**

		Inp	uts			-			Out	puts			
E	nab	le	5	Sele	ct				-	put			
GL	G1	G2	С	В	Α	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	Н	X	X	X	Н	Н	Н	Н	Н	Н	Н	Н
X	L	X	X	X	X	Н	Н	Н	Н	Н	Н	Н	Н
L	Н	L	L	L	L	L	Н	Н	Н	Н	Н	Н	Н
L	Н	L	L	L	Н	Н	L	Н	Н	Н	Н	Н	Н
L	Н	L	L	Н	L	Н	H	L	Н	Н	Н	Н	Н
L	Н	L	L	Н	Н	Н	Н	Н	L	Н	Н	Н	Н
L	Н	L	Н	L	L	Н	Н	Н	Н	L	Н	Н	Н
L	H	L	Н	L	Н	Н	Н	Н	Н	Н	L	Н	Н
L	Н	L	Н	Н	L	Н	Н	Н	Н	Н	Н	L	Н
L	Н	L	Н	Н	Н	Н	Н	Н	Н	Н	Н	Н	L
Н	Н	L	X	X	X	Ou					-	o sto	

L = Low State, H = High State, X = Don't Care

	D	M54ALS1	37	D	M74ALS1	37	
	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage		5	5.5	4.5	5	5.5	V
	2		See See	2	PACE IN		V
			0.8			0.8	V
			-0.4		and the second	-0.4	mA
	3		4			8	mA
GL	15	W.		10			ns
A, B, C	15↑			10↑			ns
A, B, C	5↑	MIL		5↑			ns
	A, B, C	Min 4.5 2 GL 15 A, B, C 15t	Min Nom  4.5 5 2  GL 15 A, B, C 151	4.5 5 5.5  2 0.8  -0.4  4 GL 15  A, B, C 151	Min Nom Max Min  4.5 5 5.5 4.5  2 2  0.8  -0.4  4  GL 15 10  A, B, C 151 101	Min Nom Max Min Nom  4.5 5 5.5 4.5 5  2 0.8 -0.4 4  GL 15 10  A, B, C 151 101	Min         Nom         Max         Min         Nom         Max           4.5         5         5.5         4.5         5         5.5           2         0.8         0.8         -0.4         -0.4           4         4         8           GL         15         10         101           A, B, C         151         101         101

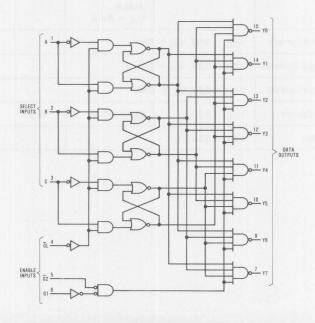
	Parameter	Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Voltage	$V_{CC} = 4.5V, I_{I} = -18mA$				-1.5	٧
VOH	High Level Output Voltage	I <sub>OH</sub> = 0.4mA		V <sub>CC</sub> -2			V
VOL	Low Level Output Voltage	$V_{CC} = 4.5V$	54/74ALS I <sub>OL</sub> = 4 mA		0.25	0.4	٧
			74ALS I <sub>OL</sub> = 8 mA		0.35	0.5	V
lį	Max High Input Current	$V_{CC} = 5.5V, V_{IH}$	= 7V			0.1	mA
lіН	High Level Input Current	$V_{CC} = 5.5V, V_{IH}$	= 2.7V			20	μΑ
IIL	Low Level Input Current	$V_{CC} = 5.5V, V_{IL}$	= 0.4V			-0.2	mA
Io	Output Drive Current	$V_{CC} = 5.5V$	$V_0 = 2.25V$	-30		-110	mA
ICC	Supply Current	$V_{CC} = 5.5V$			5	10	mA

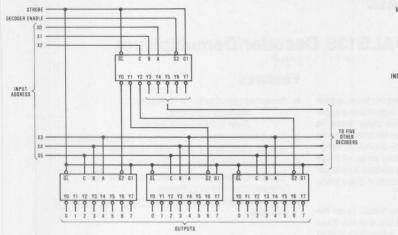
# Switching Characteristics over recommended operating free air temperature range (Note 1)

	- SARRIDARIA		DI	M54ALS1	37	DN	174ALS	137	
Parameter	From (Input)	Conditions	Min	Тур	Max	Min	Тур	Max	Unit
TPLH	A, B, C 3 Levels		3	9	20	3	9	16	ns
TPHL	of Delay		4	10	25	4	10	20	
TPLH	A, B, C 4 Levels		4	12	25	4	12	20	
TPHL	of Delay		5	13	25	5	13	20	
T <sub>PLH</sub>	G2	$V_{CC} = 4.5 \text{ to } 5.5V$ $R_L = 500 \Omega$	4	7.5	15	4	7.5	12	
T <sub>PHL</sub>		$C_L = 50 \text{ pF}.$	5	7.5	18	5	7.5	15	
TPLH	G1		5	10	21	5	10	17	
TPHL	THE DESIGNATION AND RAFE	mumumpus na 1891 janasany	5	10	19	5	10	15	dia
TPLH	GL	Bilt.	7	13	25	7	13	20	
TPHL		And And	7	13	25	7	13	20	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-3.

# **Logic Diagrams**







Preliminary

# DM54ALS138/DM74ALS138 Decoder/Demultiplexer

# **General Description**

These Schottky-clamped circuits are designed to be used in high-performance memory-decoding or data-routing applications, requiring very short propagation delay times. In high-performance memory systems these decoders can be used to minimize the effects of system decoding. When used with high-speed memories, the delay times of these decoders are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The ALS138 decodes one-of-eight lines, based upon the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented with no external inverters, and 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

This decoder/demultiplexer features fully buffered inputs, presenting only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and simplify system design.

#### **Features**

- Designed specifically for high-speed:
   Memory decoders
   Data transmission systems
- 3-to-8-line decoder incorporates 3 enable inputs to simplify cascading and/or data reception.
- Low Power Dissipation . . . 23 mW Typ.
- Switching Specification Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.

### **Absolute Maximum Ratings**

 Supply Voltage
 7V

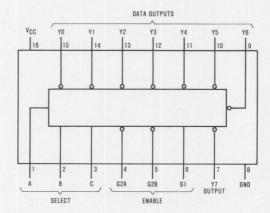
 Input Voltage
 7V

 Operating Free Air Temperature Range
 —55°C to 125°C

 DM54ALS
 —0°C to 70°C

 Storage Temperature Range
 —65°C to 150°C

### **Connection Diagram**



54ALS138 (J) 74ALS138 (J,N)

	D	M54ALS1	38	D	M74ALS1	38	
Parameter	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage	4.5	5	5.5	4.5	5	5.5	٧
High Level Input Voltage, VIH	2		The second	2	verifyets in		V
Low Level Input Voltage, VIL			0.8			0.8	V
High Level Output Current, IOH			-0.4		2 (0.0)	-0.4	mA
Low Level Output Current, IOL			4	- W. W.	5/8/34/10	8	mA

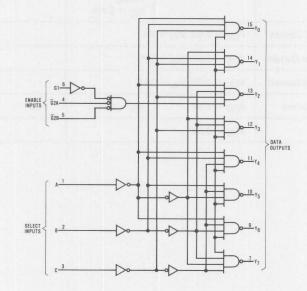
	Parameter	Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Voltage	$V_{CC} = 4.5V, I_{I} = -18mA$			Tiles	-1.5	V
VOH	High Level Output Voltage	I <sub>OH</sub> = 0.4mA		V <sub>CC</sub> -2			V
VOL	Low Level Output Voltage	$V_{CC} = 4.5V$	54/74ALS I <sub>OL</sub> = 4 mA		0.25	0.4	V
			74ALS I <sub>OL</sub> = 8 mA		0.35	0.5	٧
lj	Max High Input Current	$V_{CC} = 5.5V, V_{IH}$	= 7V			0.1	mA
ΙΗ	High Level Input Current	$V_{CC} = 5.5V, V_{IH}$	= 2.7V			20	μΑ
I <sub>IL</sub>	Low Level Input Current	$V_{CC} = 5.5V, V_{IL}$	= 0.4V			-0.2	mA
IO	Output Drive Current	V <sub>CC</sub> = 5.5V	$V_{O} = 2.25V$	-30		-110	mA
Icc	Supply Current	$V_{CC} = 5.5V$			5	10	mA

# Switching Characteristics over recommended operating free air temperature range (Note 1)

			DI	M54ALS1	138	DI	M74ALS1	38	
Parameter	From (Input)	Conditions	Min	Тур	Max	Min	Тур	Max	Unit
TPLH	A, B, C 4 Levels		7	7.5	25	7	7.5	20	ns
TPHL	of Delay		6	8	22	6	8	18	
TPLH	A, B, C 3 Levels		6	8.5	21	6	8.5	18	
TPHL	of Delay	V <sub>CC</sub> = 4.5 to 5.5V	6	7.5	21	6	8.5	18	
TPLH	Enable	$R_L = 500 \Omega$ $C_L = 50 \text{ pF}.$	4	6	15	4	6	13	
TPHL	G2	Name Party Color of the Color	5	8	19	5	8	15	
TPLH	Enable		5	8.5	20	5	8.5	17	
T <sub>PHL</sub>	G1	100	6	8	20	6	8	17	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-1.

# **Logic Diagram**





# DM54ALS151/DM74ALS151 8-Line to 1-Line **Data Selector/Multiplexer**

### **General Description**

This Data Selector/Multiplexer contains full on-chip decoding to select one-of-eight data sources as a result of a unique three-bit binary code at the Select inputs. Two complementary outputs provide both inverting and non-inverting buffer operation. A Strobe input is provided which, when at the high level, disables all data inputs and forces the Y output to the low state and the W output to the high state. The Select input buffers incorporate internal overlap features to ensure that select input changes do not cause invalid output transients.

#### **Features**

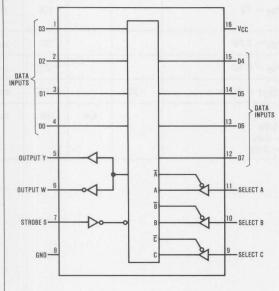
Advanced Oxide-Isolated, Ion-Implanted Schottky TTL

- Switching Performance is Guaranteed Over Full Temperature and VCC Supply Range.
- Pin and Functional Compatible with LS Family Counterpart.
- Improved Output Transient Handling Capability.

#### **Absolute Maximum Ratings**

Supply Voltage	7.0V
Input Voltage	7.0V
Operating Free Air Temperature Range	
DM54ALS151	-55°C to 125°C
DM74ALS151	0°C to 70°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature	
(Soldering, 10 seconds)	+300°C

### **Connection Diagram**



74ALS151 (J,N)

54ALS151 (J)

### **Function Table**

	Inp	uts		Outp	uts
	Select		Strobe	Y	W
С	В	Α	S		
X	X	X	Н	L	Н
L	L	L	L	D0	D0
L	L	Н	L	D1	D1
L	Н	L	L	D2	D2
L	Н	Н	L	D3	D3
Н	L	L	L	D4	D4
Н	L	Н	L	D5	D5
Н	Н	L	L	D6	D6
Н	Н	Н	L	D7	D7

H = High Level L = Low Level X = Don't Care D0 thru D7 = the level of the respective D input

		M54ALS1	51	D	51	3	
Parameter	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, VCC	4.5		5.5	4.5		5.5	V
High Level Input Voltage, VIH	2.0			2.0		BIR	V
Low Level Input Voltage, VIL			0.8	marite		0.8	V
High Level Output Current, IOH			-1.0	100 miles	alphan.	-2.6	mA
Low Level Output Current, IOL			12			24	mA

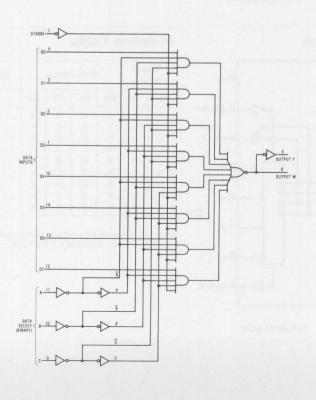
	Parameter	Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Voltage	$V_{CC} = 4.5V$ , $I_{IN}$	= -18mA		dgauhen	-1.5	V
Vон	High Level Output	$V_{CC} = 4.5V, I_{OH}$	= Max	2.4	3.2		V
BEI TO	Voltage	$IOH = -400\mu A$		V <sub>CC</sub> -2			V
VOL	Low Level Output Voltage	V <sub>CC</sub> = 4.5V	54ALS/74ALS I <sub>OL</sub> = 12mA		.25	.40	٧
	elde	Employee's	74ALS I <sub>OL</sub> = 24mA	The last	.35	.50	V
lį	Input Current at Max Input Voltage	$V_{CC} = 5.5V, V_{IN} = 7V$				100	μΑ
IIH	High Level Input Current	$V_{CC} = 5.5V, V_{IN}$	= 2.7V			20	μΑ
IIL	Low Level Input Current	$V_{CC} = 5.5V, V_{IN}$	= 0.4V			-200	μΑ
10	Output Drive Current	$V_{CC} = 5.5V, V_{OU}$	JT = 2.25V	-30		-110	mA
Icc	Supply Current	V <sub>CC</sub> = 5.5V Date Inputs = 3.0 Select Inputs = 3 Strobe Inputs = 3	.0V		6.0	10	mA

# Switching Characteristics over recommended operating free air temperature range (Note 1)

				DM54ALS151			DM74ALS151			
Parameter	From	То	Conditions	Min	Тур	Max	Min	Тур	Max	Uni
tpLH, Low to high Level Output	- Fots	Y		7.5	BTI	MA	7.5	BB #	ns	
tpHL, High to low Level Output					9.0	g II ju		9.0	le8	ns
tPLH, Low to high Level Output	Select	147			9.0			9.0	la.	ns
tPHL, High to low Level Output		W			9.5			9.5		ns
tpLH, Low to high Level Output		Y			4.0	Garden Control		4.0	in the	ns
tPHL, High to low Level Output	Dete	Y	V <sub>CC</sub> =		6.0	6(2) 87(L)	n min	6.0	many 2	ns
tPLH, Low to high Level Output	Data	vall vere	$4.5 \text{ to } 5.5 \text{V}$ $C_L = 50 \text{ pF}$		6.0	li Hode	The	6.0	100	ns
tPHL, High to low Level Output	tolisten	W	$R_L = 500 \Omega$	PHO DE	6.0			6.0	12.0	ns
tpLH, Low to high Level Output		Y			4.0	elles bi	e nave	4.0	(C) (a)	ns
tPHL, High to low Level Output	Strobe	T			5.0			5.0		ns
tpLH, Low to high Level Output	Strobe	w			4.0			4.0		ns
tPHL, High to low Level Output		VV			5.0	9.500		5.0		ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-1.

# **Logic Diagram**





Preliminary

# DM54ALS153/DM74ALS153 Dual 4-Line to 1-Line Data Selector/Multiplexer

### **General Description**

This Data Selector/Multiplexer contains full on-chip decoding to select one-of-four data sources as a result of a unique two-bit binary code at the Select inputs. Each of the two Data Selector/Multiplexer circuits have their own separate Select, Data, and Strobe inputs and a non-inverting output buffer. The Strobe inputs, when at the high level, disable their associated data inputs and force the corresponding output to the low state. The Select input buffers incorporate internal overlap features to ensure that select input changes do not cause invalid output transients.

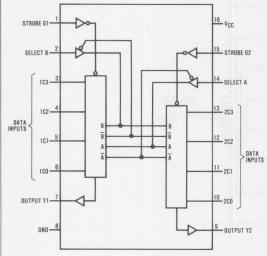
### **Absolute Maximum Ratings**

Supply Voltage	7.0V
Input Voltage	7.0V
Operating Free Air Temperature Range	
DM54ALS153	-55°C to 125°C
DM74ALS153	0°C to 70°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature	
(Soldering 10 seconds)	+300°C

#### **Features**

- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL process.
- Switching Performance is Guaranteed Over Full Temperature and V<sub>CC</sub> Supply Range.
- Pin and Functional Compatible with LS Family Counterpart.
- Improved Output Transient Handling Capability.

# Connection Diagram Function Table



74ALS153 (J,N)

54ALS153 (J)

Select in	puts A and B	are common to both	sections
H = Hig	h Level L = Lo	ow Level X = Don't	Care

	ect uts		Data Inputs			Strobe	Output
В	Α	CO	C1	C2	СЗ	G	Υ
X	X	X	X	X	X	Н	L
L	L	L	X	X	X	L	L
L	L	Н	X	X	X	L	Н
L	Н	X	L	X	X	L	L
L	Н	X	Н	X	X	L	Н
Н	L	X	X	L	X	L	L
Н	L	X	X	Н	X	L	Н
Н	Н	X	X	X	L	L	L
Н	Н	X	X	X	Н	L	Н

	D	M54ALS1	53	D	53	11-14	
Parameter	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, VCC	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, VIH	2			2	potenti lipote		V
Low Level Input Voltage, VIL			0.8		W.S. Mr.S.	0.8	V
High Level Output Current, IOH	1402 4		-1.0		gtuð Imm	-2.6	mA
Low Level Output Current, IOL			12		pub leve	24	mA

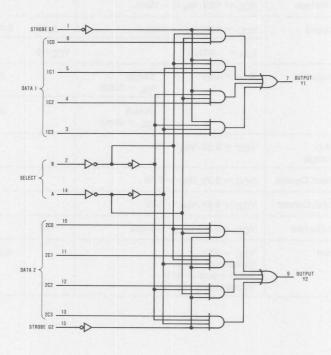
	Parameter	Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Voltage	$V_{CC} = 4.5V, I_{IN}$	= -18mA			-1.5	V
Vон	High Level Output	$V_{CC} = 4.5V, I_{OH}$	= Max	2.4	3.2		V
	Voltage	$I_{OH} = -400\mu A$	V <sub>CC</sub> -2			V	
VOL	Low Level Output Voltage	$V_{CC} = 4.5V$	54ALS I <sub>OL</sub> = 12mA		.25	.40	V
		74ALS IOL = 24mA		.35	.50	V	
lı	Input Current at Max Input Voltage	V <sub>CC</sub> = 5.5V, V <sub>IN</sub> = 7V				100	μΑ
ΙΗ	High Level Input Current	$V_{CC} = 5.5V, V_{IN}$	= 2.7V			20	μΑ
IIL	Low Level Input Current	$V_{CC} = 5.5V, V_{IN}$	= 0.4V			-200	μΑ
IO	Output Drive Current	V <sub>CC</sub> = 5.5V, V <sub>OUT</sub> = 2.25V		-30		-110	mA
lcc	Supply Current	V <sub>CC</sub> = 5.5V Date Inputs = 3.0V Select Inputs = 3.0V Strobe Inputs = 3.0V			6.3	10	mA

# Switching Characteristics over recommended operating free air temperature range (Note 1)

			Conditions	DM54ALS153			DM74ALS153			
Parameter	From	То		Min	Тур	Max	Min	Тур	Max	Unit
tpLH, Low to high Level Output		Select Y	V <sub>CC</sub> = 4.5 to 5.5V C <sub>L</sub> = 50 pF R <sub>L</sub> = 500 Ω		7.5			7.5		ns
t <sub>PHL</sub> , High to low Level Output	Select				9.0			9.0		ns
tpLH, Low to high Level Output					4.0			4.0		ns
tpHL, High to low Level Output	Data	Y			6.0	- 14		6.0		ns
tpLH, Low to high Level Output	Church	Strobe Y			4.0			4.0		ns
tpHL, High to low Level Output	Strobe				5.0			5.0		ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-1.

# **Logic Diagram**



# DM54ALS/DM74ALS157,158 Quad 2-Line to 1-Line Data Selectors/Multiplexers

#### **General Description**

These data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The ALS 157 presents true data whereas the ALS 158 presents inverted data to minimize propagation delay time.

#### **Features**

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin for Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.

- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.
- Expand any data input point.
- Multiplex dual data buses.
- General four functions of two variables (one variable is common).
- Source programmable counters.

### **Absolute Maximum Ratings**

 Supply Voltage
 7V

 Input Voltage
 7V

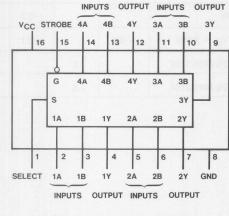
 Operating Free Air Temperature Range
 —55°C to 125°C

 DM54ALS
 —0°C to 70°C

 DM74ALS
 0°C to 70°C

 Storage Temperature Range
 —65°C to 150°C

### **Connection Diagram**



54ALS157 (J) 74ALS157 (J,N)

54ALS158 (J) 74ALS158 (J,N)

#### **Function Table**

	Inputs	Output Y				
Strobe	Select	Α	В	ALS157	ALS158	
Н	X	X	X	L	Н	
L	L	L	X	L	Н	
L	L	Н	X	Н	L	
L	Н	X	L	L	Н	
L	Н	X	Н	Н	L L	

H = High Level, L = Low Level, X = Don't Care

	DM	54ALS157	,158	DM			
Parameter	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, V <sub>CC</sub>	4.5	5	5.5	4.5	5	5.5	٧
High Level Input Voltage, VIH	2			2			٧
Low Level Input Voltage, VIL	artista (a. 1911)		0.8	entire.	lignor.	0.8	V
High Level Output Current, IOH		A STATE OF	-1.0		- Selak	-2.6	mA
Low Level Output Current, IOL			12		Constant	24	mA

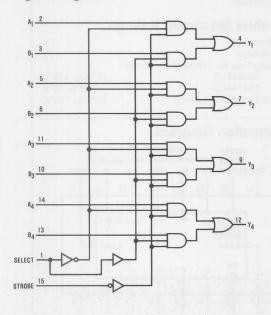
	Parameter	Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Voltage	V <sub>CC</sub> = 4.5V, I <sub>I</sub> =	-18mA			-1.5	V
Vон	High Level Output Voltage	$I_{OH} = -0.4$ mA	$I_{OH} = -0.4$ mA				V
VOL	Low Level Output Voltage	V <sub>CC</sub> = 4.5V 54/74ALS I <sub>OL</sub> = 12 mA		Call Park Balls	0.25	0.4	V
			74ALS I <sub>OL</sub> = 24 mA		0.35	0.5	V
lį .	Max High Input Current	$V_{CC} = 5.5V, V_{IH}$	$V_{CC} = 5.5V, V_{IH} = 7V$			0.1	mA
IIH	High Level Input Current	$V_{CC} = 5.5V, V_{IH}$	= 2.7V			20	μΑ
IIL	Low Level Input Current	$V_{CC} = 5.5V, V_{IL}$	= 0.4V			-0.2	mA
10	Output Drive Current	$V_{CC} = 5.5V$	$V_0 = 2.25V$	-30		-110	mA
Icc	Supply Current	V <sub>CC</sub> = 5.5V	54/74ALS157		7.8		mA
			54/74ALS158	W. A	2.3		mA

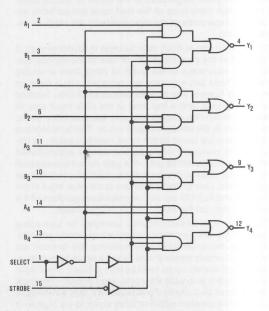
# Switching Characteristics over recommended operating free air temperature range (Note 1)

		From	То	TTCIH	DM54	4ALS15	7,158	DM7	4ALS15	7,158											
Parameter		(Input)	(Output)	Conditions	Min	Тур	Max	Min	Тур	Max	Unit										
T <sub>PLH</sub> ,	157			na mair	1.7	3.5	8.7	1.7	3.5	7.0											
Propagation Delay Time. Low to High Level Output	158	Data	Y	V <sub>CC</sub> =	1.7	3.5	8.7	1.7	3.5	7.0											
T <sub>PHL</sub> ,	157			$4.5 \text{ to } 5.5 \text{V}$ $C_L = 50 \text{ pF}$ $R_L = 500 \Omega$	2.5	5.0	12.5	2.5	5.0	10.0											
Propagation Delay Time. High to Low Level Output	158				2.5	5.0	12.5	2.5	5.0	10.0											
T <sub>PLH</sub> ,	157	knotthi	105 681 YEL	Antonia trapo	3.0	6.0	15.0	3.0	6.0	12.0											
Propagation Delay Time. Low to High Level Output	158	Strobe	Y	retains	3.0	6.0	15.0	3.0	6.0	12.0	ns										
TPHL,	157	estus Lucias	March an	Crimical and any	3.2	6.5	16.2	3.2	6.5	13.0											
Propagation Delay Time. High to Low Level Output	158		me ilia	control of 16		3.1	6.2	2 15.5	3.1	6.2	12.4										
TPLH,	157					ment -			1000			nobel 1	0.0010	Total Till	100019	more :	3.0	6.0	15.0	3.0	6.0
Propagation Delay Time. Low to High Level Output	158	Select	Y	S. I Diver	3.0	6.0	15.0	3.0	6.0	12.0											
TPHL,	157	Laherr XI Etalogo	esen oa e Permaki	Maria Maria	3.2	6.5	16.2	3.2	6.5	13.0											
Propagation Delay Time. High to Low Level Output	158		rij -jestana		3.1	6.2	15.5	3.1	6.2	12.4											

NOTE 1: See notes pg. 1-iii, figures pg. 3-1.

# **Logic Diagrams**





National Semiconductor

Preliminary

# DM54ALS/DM74ALS160,161,162,163 Synchronous Four-Bit Counters

#### **General Description**

These synchronous presettable counters feature an internal carry look ahead for application in high speed counting designs. The ALS160 and ALS162 are four-bit decade counters, while the ALS161 and ALS163 are four-bit binary counters. The ALS160 and ALS161 clear asynchronously, while the ALS162 and ALS163 clear synchronously. The carry output is decoded to prevent spikes during normal counting mode of operation. Synchronous operation is provided by having all flip-flops clocked simultaneously so that outputs change coincident with each other when so instructed by count enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flipflops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable, that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with set up data after the next clock pulse regardless of the levels of enable input. Low to high transitions at the load input are perfectly acceptable regardless of the logic levels on the clock or enable inputs.

The ALS160 and ALS161 clear function is asynchronous. A low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of clock, load or enable inputs. These two counters are provided with a clear on power-up feature. The ALS162 and ALS163 clear function is synchronous; and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of enable inputs. This synchronous clear allows the count length to be modified easily, as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to all low outputs. Low to high transitions at the clear input of the ALS162 and ALS163 are also permissible regardless of the levels of logic on the clock, enable or load inputs.

The carry look ahead circuitry provides for cascading counters for n bit synchronous application without additional gating. Instrumental in accomplishing this function are two count-enable inputs (P and T) and a ripple carry output. Both count-enable inputs must be high to count. The T input is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high level output pulse with a duration approximately equal to the high level portion of QA output. This high level overflow ripple carry pulse can be used to enable successive cascaded stages. High to low level transitions at the enable P or T inputs of the ALS160 through ALS163, may occur regardless of the logic level on the clock.

The ALS160 through ALS163 feature a fully independent clock circuit. Changes made to control inputs (enable P or T, or load) that will modify the operating mode will have no

effect until clocking occurs. The function of the counter (whether enabled, disabled, loading or counting) will be dictated solely by the conditions meeting the stable set-up and hold times.

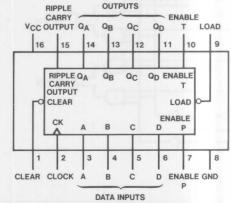
#### **Features**

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Shottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.
- Synchronously programmable.
- Internal look ahead for fast counting.
- Carry output for n-bit cascading.
- Synchronous counting.
- Load control line.
- ESD inputs.

### **Absolute Maximum Ratings**

Supply Voltage 7V
Input Voltage 7V
Operating Free Air Temperature Range
DM54ALS -55°C to 125°C
DM74ALS 0°C to 70°C
Storage Temperature Range -65°C to 150°C

### **Connection Diagram**



54ALS160 (J) 74ALS160 (J,N) 54ALS161 (J) 74ALS161 (J,N) 54ALS162 (J) 74ALS162 (J,N) 54ALS163 (J) 74ALS163 (J,N)

			DM54ALS 0,161,162,		16	DM74ALS 0,161,162,		
Parameter		Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage	14-5aV   14-5aV	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage	, VIH	2			2	mile in imp		V
Low Level Input Voltage,	VIL	1301		0.8			0.8	V
High Level Output Curre	nt, IOH	301		-0.4			-0.4	mA
Low Level Output Currer	nt, I <sub>OL</sub>	WT -	Apr. MLI	4		None in	8	mA
Clock Frequency, fCLOC	K	0	NE I	50	0	Discontinues	55	МН
tsetup, Set-up time	Data; A, B, C, D	12	6		12	6		ns
	En P, En T	16	8	, riad	16	8		ns
	Load	16	8	m pay	16	8		ns
AND DE CO	Clear (Only for 162 & 163)	20	10	- 64%	20	10		ns
Set-up 1 (Only for 160 & 161)	Clear	8	4	es unio	8	4	eÓ par	ns
thold, Hold time	Data; A, B, C, D	0	-3		0	-3	10	ns
	En P, En T	0	-3		0	-3		ns
	Load	0	-4		0	-4		ns
	Clear (Only for 162 & 163)	0	-7		0	-7		ns
Hold 0 (Only for 160 & 161)	Clear	0	-4	1 1150	0	-4		ns
Width of Clock or Clear F	Pulse, TW	10			9		Part I	ns

# Electrical Characteristics over recommended operating free air temperature range (Note 1)

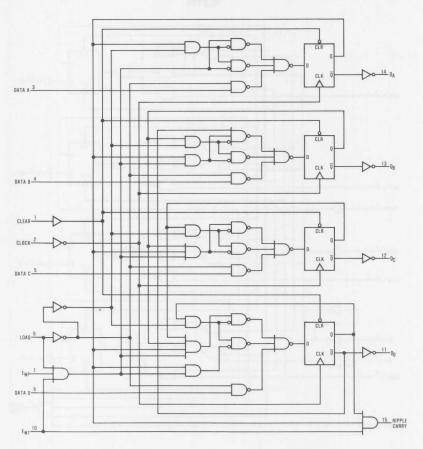
	Parameter	Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Voltage	$V_{CC} = 4.5V$ , $I_I =$	-18mA			-1.5	V
Vон	High Level Output Voltage	$I_{OH} = -0.4$ mA		V <sub>CC</sub> -2			V
VOL	Low Level Output Voltage	V <sub>CC</sub> = 4.5V	54/74ALS I <sub>OL</sub> = 4mA		0.25	0.4	٧
	Age	5.0-	74ALS I <sub>OL</sub> = 8mA	600	0.35	0.5	٧
l <sub>l</sub>	Max High Input Current	$V_{CC} = 5.5V, V_{IH}$	= 7V		(, A) = ( )	0.1	mA
lін	High Level Input Current	V <sub>CC</sub> = 5.5V V <sub>IH</sub> = 2.7V	DATA, CLR, CLK, EN P LOAD, EN T	- Limita		20	μΑ
IIL	Low Level Input Current	V <sub>CC</sub> = 5.5V, V <sub>IL</sub> DATA, CLR, CLK	= 0.4V , EN P, LOAD, ENT	D.B.A		-0.2	mA
10	Output Drive Current	V <sub>CC</sub> = 5.5V	$V_0 = 2.25V$	-30		-110	mA
Icc		V <sub>CC</sub> = 5.5V		1000	11	16	mA

# Switching Characteristics over recommended operating free air temperature range (Note 1)

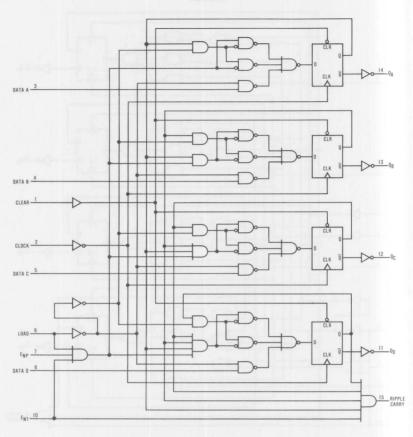
					DM54AL9	_		DM74AL9		
Parameter	From	То	Conditions	Min	Тур	Max	Min	Тур	Max	Unit
fmax, Max. clock freq.				50	90		55	90		MHZ
TPLH, Propagation delay time. Low to high level output.	Clock	Ripple		4	14	25	4	14	23	ns
TPHL, Propagation delay time. High to low level output.		Carry								
With Load High				3	10	18	3	10	17	ns
With Load Low				5	15	27	5	15	25	ns
TPLH, Propagation delay time. Low to high level output.	Clock	Any Q	V <sub>CC</sub> = 4.5	3	9	16	3	9	15	ns
TPHL, Propagation delay time. High to low level output.	_ Clock	7.iiy Q	to 5.5V $R_L = 500 \Omega$ $C_L = 50 pF$	3	10	19	3	10	17	ns
TPLH, Propagation delay time. Low to high level output.	En T	Ripple		2	5	9	2	5	8	ns
TPHL, Propagation delay time. Low to high level output.		Carry		2	6	11	2	6	10	ns
TPHL, Propagation delay time. High to low level output.	Clear	Any Q		4	12	22	4	12	20	ns

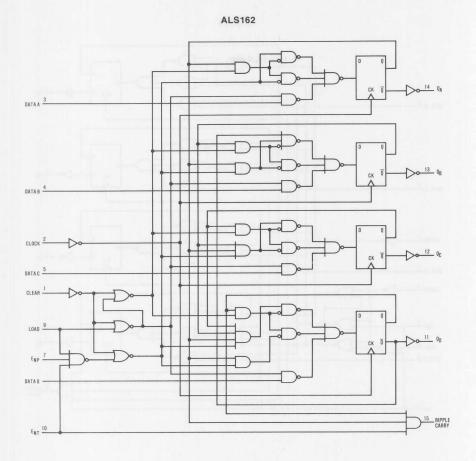
NOTE 1: See notes pg. 1-iii, figures pg. 3-3.



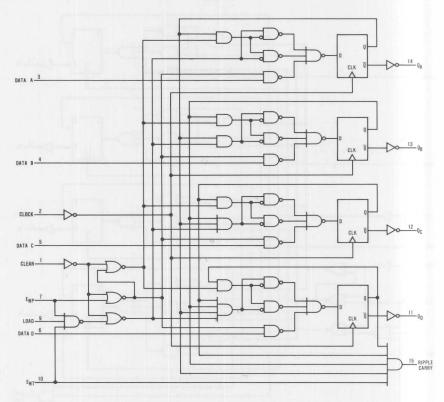


## ALS161





#### ALS163





# DM54ALS/DM74ALS168,169 Synchronous Four Bit Up/Down Counters

### **General Description**

These synchronous presettable counters feature an internal carry look ahead for cascading in high speed counting applications. The ALS168 is a four-bit decade up/down counter and the ALS169 is a four-bit binary up/down counter. The carry output is decoded to prevent spikes during normal mode of counting operation. Synchronous operation is provided so that outputs change coincident with each other when so instructed by count enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive going) edge of clock input waveform.

These counters are fully programmable; that is, the outputs may each be preset either high or low. The load input circuitry allows loading with carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry permits cascading counters for n-bit synchronous applications without additional gating. Both count enable inputs ( $\vec{P}$  and  $\vec{T}$ ) must be low to count. The direction of the count is determined by the level of the up/down input. When the input is high, the counter counts up; when low, it counts down. Input  $\vec{T}$  is fed forward to enable the carry outputs. The carry output thus enabled will produce a low level output pulse with a duration approximately equal to the high portion of the QA output when counting up, and approximately equal to the low portion of the QA output when counting down. This low level overflow carry pulse can be used to enable successively cascaded stages. Transitions at the enable  $\vec{P}$  or  $\vec{T}$  inputs are allowed regardless of the level of the clock input.

The control functions for these counters are fully synchronous. Changes at control inputs (enable P, enable T, load, up/down) which modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

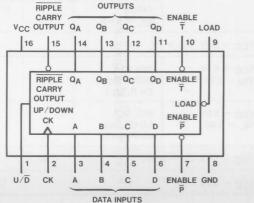
#### **Features**

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin-for-Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.
- Synchronously Programmable.
- Internal Look Ahead for Fast Counting.
- Carry Output for N-bit Cascading.
- Synchronous Counting.
- Load Control Line.
- ESD Inputs.

# **Absolute Maximum Ratings**

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS	-55°C to 125°C
DM74ALS	0°C to 70°C
Storage Temperature Range	-65°C to 150°C

### **Connection Diagram**



54ALS168 (J) 74ALS168 (J,N)

54ALS169 (J) 74ALS169 (J,N)

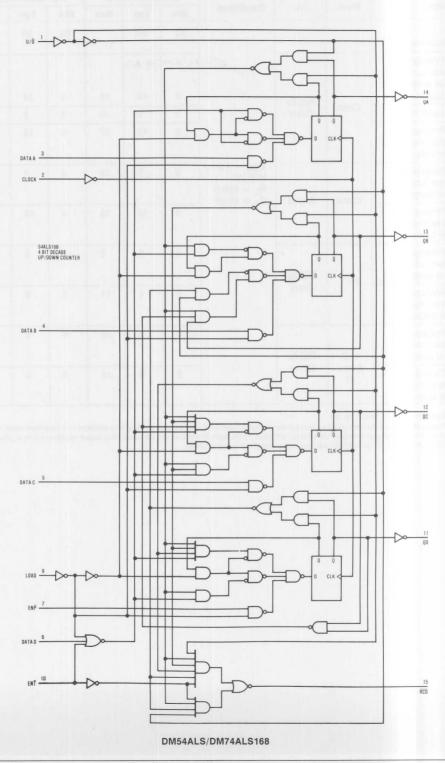
		DM	54ALS168	,168	DM	74ALS168	,169	
Parameter		Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage	, V <sub>IH</sub>	2	NgU	NE TU	2	Jone	PM)	V
Low Level Input Voltage	, VIL			0.8			0.8	V
High Level Output Curre	nt, IOH		n in elder	-0.4			-0.4	mA
Low Level Output Currer	nt, IOL			4			8	mA
Clock Frequency, fCLOC	СК	0		50	0		55	МН
tsetup, Set-up time	Data; A, B, C, D	12	6	ingil outla populari los trusco.	12	6		ns
	En P, En T	16	8	Sila micara	16	8		ns
	Load	16	8		16	8		ns
armines, spinisspin-on	U/D	20	10		20	10		ns
thold, Hold time	Data; A, B, C, D	0	-3	off and S tiple officer	0	-3		ns
	En P, En T	0	-3	m) we	0	-3	de n	ns
	Load	0	-4		0	-4		ns
	U/D	0	-4	rociums an	0	-4		ns
Width of Clock Pulse, Ty	V	10	and the		9	TV TEAS		ns

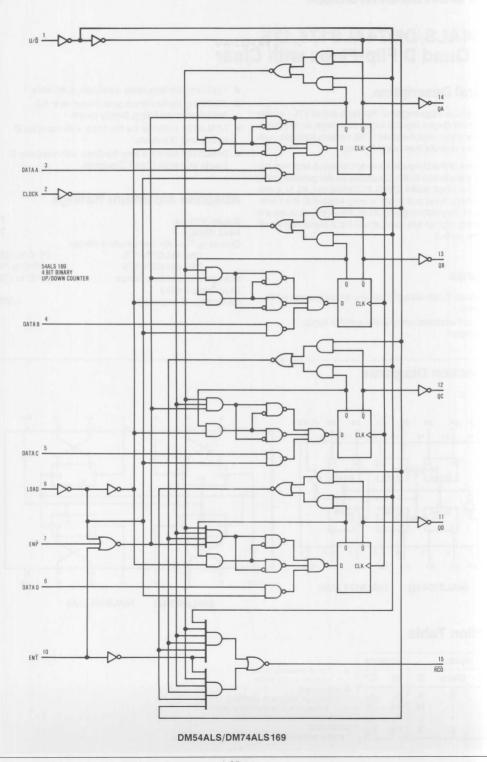
	Parameters	Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Voltage	V <sub>CC</sub> = 4.5V, I <sub>I</sub> =	-18mA			-1.5	V
Vон	High Level Output Voltage	$I_{OH} =4mA$		V <sub>CC</sub> -2	An And	10 Aug.	V
VOL	Low Level Output Voltage	V <sub>CC</sub> = 5.5V	54/74ALS I <sub>OL</sub> = 4 mA	grami	0.25	0.4	V
			74ALS I <sub>OL</sub> = 8 mA	ALTERNATION OF	0.35	0.5	V
IĮ.	Max High Input Current	$V_{CC} = 5.5V, V_{IH}$	= 7V			0.1	mA
ΊΗ	High Level Input Current	V <sub>CC</sub> = 4.5V V <sub>IH</sub> = 2.7V	U/D, CLK, LOAD, Data, EN P, EN T			20	μΑ
IĮĽ	Low Level Input Current	V <sub>CC</sub> = 5.5V V <sub>IL</sub> = 0.4V	U/D, CLK, LOAD, Data, EN P, EN T	MARK SUL		-0.2	mA
10	Output Drive Current	$V_{CC} = 5.5V, V_O$	= 2.25V	-30		-110	mA
Icc		$V_{CC} = 5.5V$		R5 - 3	13	20	mA

				DM5	4ALS16	8,169	DM7	4ALS168	8,169	
Parameter	From	То	Conditions	Min	Тур	Max	Min	Тур	Max	Unit
fmax, Max. clock freq.				50	90		50	90	17-17	MHz
TPLH, Propagation delay time. Low to high level output. With Load Low		Ripple		4	14	25	4	14	23	ns
With Load High	Clock	Carry		3	8	16	3	8	14	ns
TPHL, Propagation delay time. High to low level output.				5	15	27	5	15	25	ns
TPLH, Propagation delay time. Low to high level output.	Clock	Any Q	$V_{CC} = 4.5$ to 5.5V $R_{L} = 500 \Omega$ $C_{I} = 50 pF$	3	9	16	3	9	15	ns
TPHL, Propagation delay time. High to low level output.	_ CIOCK	Ally Q	OL = 30 pi	3	10	19	3	10	17	ns
TPLH, Propagation delay time. Low to high level output.	En T	Ripple		2	5	9	2	5	8	ns
TPHL, Propagation delay time. High to low level output.		Carry		2	6	11	2	6	10	ns
TPLH, Propagation delay time. Low to high level output.	U/D	Ripple	-0	6	9	18	6	9	16	ns
TPHL, Propagation delay time. High to low level output.	(Note 2)	Carry		6	9	18	6	9	16	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-3.

NOTE 2: Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0), the ripple carry output transition will be in phase. If the count is maximum (9 for ALS168 or 15 for ALS169), the ripple carry output will be out of phase.





Preliminary



# DM54ALS/DM74ALS174,175 Hex/Quad D Flip-Flops with Clear

#### **General Description**

These positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. Both have an asynchronous clear input, and the quad (175) version features complementary outputs from each flip-flop.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

#### **Features**

- Advanced Oxide-Isolated Ion-Implanted Schottky TTL Process.
- Pin and Functional compatible with LS family counterpart.

- Typical clock frequency maximum is 80 MHz.
- Switching performance guaranteed over full temperature and V<sub>CC</sub> supply range.
- 54ALS174 contains six flip-flops with separate D inputs and Q outputs.
- 54ALS175 contains four flip-flops with separate D inputs and both Q and Q outputs.

### **Absolute Maximum Ratings**

 Supply Voltage
 7.0V

 Input Voltage
 7.0V

 Operating Free Air Temperature Range
 DM54ALS174/175
 -55°C to 125°C

 DM74ALS174/175
 0°C to 70°C

 Storage Temperature Range
 -65°C to 150°C

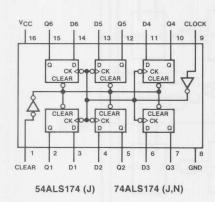
 Lead Temperature
 -65°C to 150°C

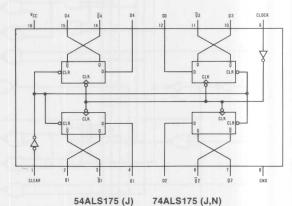
+300°C

(Soldering, 10 seconds)

T300 C

## **Connection Diagrams**





#### **Function Table**

	Inputs		Out	puts
Clear	Clock	D	Q	Q*
L	X	X	L	L
Н	1	Н	Н	Н
Н	1	L	L	L
Н	L	X	Q <sub>0</sub>	$\overline{Q}_0$

H = high level (steady state)L = low level (steady state)

don't care

 $\uparrow=$  transition from low to high level  ${\rm Q}_0=$  the level of Q before the indicated steady-state input conditions were established.

\* applies to 54ALS175/74ALS175 only

	DM	54ALS174	,175	DM	74ALS174	,175	
Parameter	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, VCC	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, VIH	2	A Salata Sal		2			V
Low Level Input Voltage, VIL			0.8		to the Co	0.8	V
High Level Output Current, IOH			-400			-400	mA
Low Level Output Current, IOL			4	H H	1.450	8	m/
Pulse Width, t <sub>W</sub> Clock			102 F				ns
Clear							
Setup Time, tSETUP Data Input					i mid		ns
Clear Inactive State							
Hold Time, tHOLD Data Input	0			0	Em		ns
Clear Active State	0		all I	0			

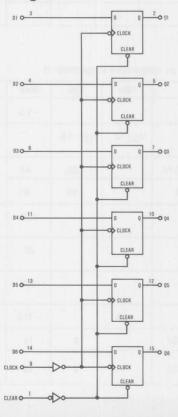
	Parameter	Conditions			Min	Тур	Max	Unit
VIK	Input Clamp Voltage	V <sub>CC</sub> = 4.5V I	IN = -18mA				-1.5	V
VOH	High Level Output Voltage	V <sub>CC</sub> = 4.5V I	$OH = -400\mu A$		V <sub>CC</sub> -2	V <sub>CC</sub> -1.6		V
VOL	Low Level Output	$V_{CC} = 4.5V$	$I_{OL} = 4mA$	DM54/74		.25	.40	٧
	Voltage		I <sub>OL</sub> = 8mA	DM74		.35	.50	
lj i	Input Current at Max Input Voltage	$V_{CC} = 5.5V,$	$V_{IN} = 7V$				100	μΑ
ΊΗ	High Level Input Current	V <sub>CC</sub> = 5.5V,	V <sub>IN</sub> = 2.7V		EARL		20	μΑ
IIL	Low Level Input Current	$V_{CC} = 5.5V,$	V <sub>IN</sub> = 0.4V				-200	μΑ
IO	Output Drive Current	$V_{CC} = 5.5V,$	V = 2.25V		-30		-110	mA
Icc	Supply Current	V <sub>CC</sub> = 5.5V		ALS174		8	14	mA
	distantive and the second	Clock = 3.0V Clear = .4V D Inputs = 3.1	0V	ALS175		6	10	

## Switching Characteristics over recommended operating free air temperature range (Note 1)

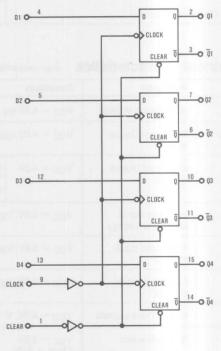
	ATT BYES	54	ALS174,1	75	74	ALS174,1	75	
Parameter	Conditions	Min	Тур	Max	Min	Тур	Max	Unit
f <sub>MAX</sub> , Maximum Clock Frequency	$R_L = 500\Omega$ $C_L = 50pF$		80			80		MHz
tp <sub>LH</sub> , Propagation Delay Time, Low to high Level Output From Clear (175 Only)	$R_{L} = 500 \Omega$ $C_{L} = 50pF$		10			10		ns
tp <sub>HL</sub> , Propagation Delay Time, High to low Level Output From Clear	$R_L = 500 \Omega$ $C_L = 50pF$		11		MI	11	and the	ns
tp <sub>LH</sub> , Propagation Delay Time, Low to high Level Output From Clock	$R_{L} = 500 \Omega$ $C_{L} = 50pF$		9			9		ns
tp <sub>HL</sub> , Propagation Delay Time, High to low Level Output From Clock	$R_L = 500 \Omega$ $C_L = 50pF$		10			10	a corto	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-3.

# **Logic Diagrams**



54ALS174/74ALS174



54ALS175/74ALS175



# DM54ALS/DM74ALS240,241,242,243,244 TRI-STATE® Bus Drivers/Receivers

### **General Description**

This family of Advance Low Power Schottky TRI-STATE Bus circuits are designed to provide either bidirectional or unidirectional buffer interface in Memory, Microprocessor, and Communication Systems. The output characteristics of the circuits have low impedance sufficient to drive terminated transmission lines down to 133 ohms. The input characteristics of the circuits likewise have a high impedance so it will not significantly load the transmission line. The package contains eight TRI-STATE buffers organized with four buffers having a common TRI-STATE enable gate. The ALS240, 241 and 244 are eight wide in a 20 pin package, and may be used as a 4 wide bidirectional or eight wide unidirectional. The ALS242 and 243 are organized four wide bidirectional in a 14 pin package. The buffer selection includes inverting and non-inverting, with enable or disable TRI-STATE control. The TRI-STATE circuitry contains a feature that maintains the buffers in TRI-STATE until the power supply (VCC) is greater than 3V. This feature prevents the buffers from glitching the system bus during power up or down.

#### **Features**

- Advanced Low Power Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Improved Switching Performance with Less Power Dissipation compared with 54/74ALS Counterpart.
- Functional and Pin Compatible with 54/74LS Counterpart.
- Switching Response Specified Into 500 ohm and 50pF.
- Low Level Drive Current 74ALS-1 48ma, 74ALS 24ma, 54ALS 12ma
- Glitch Free Bus During Power Up/Down.
- Specified to Interface with CMOS at VOH = VCC 2V.

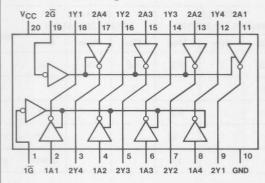
### **Absolute Maximum Ratings**

Supply Voltage, V<sub>CC</sub> 7.0V
Input Voltage 7.0V
Operating Free Air Temperature Range

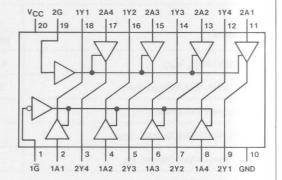
Storage Temperature Range Lead Temperature (Soldering, 10 seconds)

+300°C

# **Connection Diagrams**

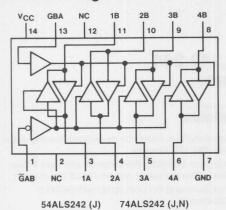


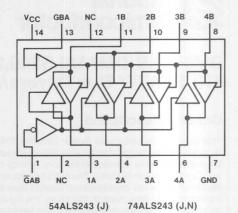
54ALS240 (J) 74ALS240 (J,N)

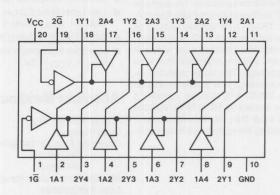


54ALS241 (J) 74ALS241 (J,N)

# **Connection Diagrams**







54ALS244 (J) 74ALS244 (J,N)

# **Recommended Operating Conditions**

Parameter	DM54ALS 240,241,242,243,244			DM74ALS 240,241,242,243,244			
	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, VCC	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, VIH	2			2			V
Low Level Input Voltage, VIL			0.8			0.8	V
High Level Output Current, IOH			-12			-15	mA
Low Level Output Current, IOL			12			12/48*	mA

<sup>\*</sup> Applies to 74ALS-1 options.

	Parameter	Conditions	Min	Тур	Max	Unit
VIK	Input Clamp Voltage	$V_{CC} = 4.5V$ , $I_{IN} = -18mA$			-1.5	٧
Vон	High Level Output Voltage	$V_{CC} = 4.5V, I_{OH} = -3mA$ $V_{CC} = 4.5V, I_{OH} = -15mA$ $I_{OH} = -400\mu A$	2.4 2.0 V <sub>CC</sub> -2	3.2 2.3	Medical abberts	V V V
VOL	Low Level Output Voltage	V <sub>CC</sub> = 4.5V I <sub>OL</sub> = 12mA 54/74 I <sub>OL</sub> = 24mA 74 I <sub>OL</sub> = 48mA 74-1		.25 .35 .35	.40 .50 .50	V V V
lı	Input Current at Max Input Voltage	$V_{CC} = 5.5V, V_{IN} = 7V$			100	μΑ
liH	High Level Input Current	$V_{CC} = 5.5V, V_{IN} = 2.7V$		or on	20	μΑ
IIL	Low Level Input Current	$V_{CC} = 5.5V, V_{IN} = 0.4V$		eig	-200	μΑ
Гохн	High Level TRI-STATE® Output Current	V <sub>CC</sub> = 5.5V, V = 2.7V		alg	20	μΑ
lozL	Low Level TRI-STATE Output Current	$V_{CC} = 5.5V, V = .4V$		9-10	-20	μΑ
10	Output Drive Current	$V_{CC} = 5.5V, V_{OUT} = 2.25V$	-30		-110	mA
Icc	Supply Current	V <sub>CC</sub> = 5.5V 54/74ALS240 Outputs High Outputs Low TRI-STATE		4.7 10.6 11.7		mA
lcc	Supply Current	V <sub>CC</sub> = 5.5V 54/74ALS241 Outputs High Outputs Low TRI-STATE		8.0 13.9 15.1		mA
lcc	Supply Current	V <sub>CC</sub> = 5.5V 54/74ALS242 A Port Outputs High A Port Outputs Low TRI-STATE		HER ST SE		mA
Icc	Supply Current	V <sub>CC</sub> = 5.5V 54/74ALS243 A Port Outputs High A Port Outputs Low TRI-STATE		94.5		mA
Icc	Supply Current	V <sub>CC</sub> = 5.5V 54/74ALS244 Outputs High Outputs Low TRI-STATE		7.6 13.5 14.8		mA

Parameter	Circuit		74ALS			54ALS		
(Propagation Delay Time)	Configuration	Min	Тур	Max	Min	Тур	Max	Unit
TPLH, Low-to-High Level Output			3.2	334		3.2		ns
TPHL, High-to-Low Level Output	ALS 240, 242		2.0			2.0		ns
TPLH, Low-to-High Level Output			4.0			4.0		ns
TPHL, High-to-Low Level Output	ALS 241, 243, 244		4.5			4.5		ns
TPZL, Output Enable to Low Level			7.2			7.2		ns
FPZH, Output Enable to High Level			5.5			5.5		ns
From Low Level	——————————————————————————————————————		4.5			4.5		ns
TPHZ, Output Disable From High Level	ALS 240, 242		3.5			3.5		ns
FPZL, Output Enable to Low Level FPZH, Output Enable to	<b>→</b>		9.2			9.2		ns
High Level  FPLZ, Output Disable			7.0	257	Thorn.	7.0		ns
From Low Level  TPHZ. Output Disable	——————————————————————————————————————	Lain ag	5.0	and the		5.0	i i	ns
From High Level	ALS 242		3.5	in the state of		3.5		ns
TPZL, Output Enable to Low Level TPZH, Output Enable to		DET IS	8.5			8.5		ns
High Level TPLZ, Output Disable			6.2			6.2		ns
From Low Level TPHZ, Output Disable		THE STATE OF	5.0			5.0		ns
From High Level	ALS 241, 243, 244	27.1915	3.5	19 A		3.5		ns
TPZL, Output Enable to Low Level TPZH, Output Enable to			9.2	Harry L.		9.2		ns
High Level TPLZ, Output Disable			7.0			7.0		ns
From Low Level TPHZ, Output Disable			5.0			5.0		ns
From High Level	ALS 241, 242		3.5	197		3.5		ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-2.

NOTE 2: Switching characteristic conditions are  $V_{CC}=4.5V$  to 5.5V,  $R_{L}=500\Omega$ ,  $C_{L}=50pF$ 

## DM54ALS251/DM74ALS251 TRI-STATE® 8-Line to 1-Line Data Selector/Multiplexer

#### **General Description**

This Data Selector/Multiplexer contains full on-chip decoding to select one-of-eight data sources as a result of a unique three-bit binary code at the Select inputs. Two complementary outputs provide both inverting and non-inverting buffer operation. An Output Control input is provided which, when at the high level, places both outputs in the high impedance Off state. In order to prevent bus access conflicts, output disable times are shorter than output enable times. The Select input buffers incorporate internal overlap features to ensure that select input changes do not cause invalid output transients.

#### **Features**

- Advanced Oxide-Isolated Ion-Implanted Schottky TTL Process.
- Switching Performance is Guaranteed Over Full Temperature and V<sub>CC</sub> Supply Range.

- Pin and Functional Compatible with LS Family Counterpart.
- Improved Output Transient Handling Capability.
- Output Control Circuitry Incorporates Power-Up Tri-State Feature.

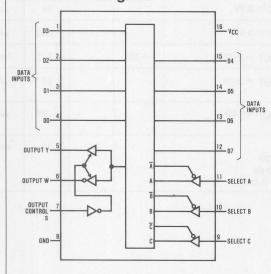
#### **Absolute Maximum Ratings**

Supply Voltage, V<sub>CC</sub>
Input Voltage
Operating Free Air Temperature Range
DM54ALS251
DM74ALS251
O°C to 70°C
Storage Temperature Range
Lead Temperature
(Soldering, 10 seconds)

7.0V
-55°C to 125°C
0°C to 70°C
+150°C

## **Connection Diagram**

54ALS251 (J)



74ALS251 (J,N)

#### **Function Table**

	Inp	uts		Outputs		
	Select		Strobe			
С	В	Α	S	Υ	W	
X	X	X	Н	Z	Z	
L	L	L	L	D0	DO	
L	L	Н	L	D1	D1	
L	Н	L	L	D2	D2	
L	Н	Н	L	D3	D3	
Н	L	L	L AND	D4	D4	
Н	L	Н	L	D5	D5	
Н	Н	L	L	D6	D6	
Н	Н	Н	L	D7	D7	

H = High Logic Level, L = Low Logic Level, X = Don't Care

Z = High Impedance (Off)

D0 thru D7 = The Level of the Respective D Input

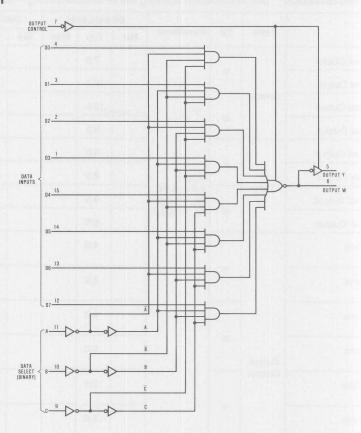
	0	M54ALS2	51	D			
Parameter	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, VCC	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, VIH	2			2			٧
Low Level Input Voltage, VIL			0.8			0.8	٧
High Level Output Current, IOH			-1.0			-2.6	mA
Low Level Output Current, IOL			12			24	mA

	Parameter	Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Voltage	$V_{CC} = 4.5V$ , $I_{IN} =$	= -18mA			-1.5	V
VOH	High Level Output	$V_{CC} = 4.5V, I_{OH}$	= Max	2.4	3.2	1	٧
	Voltage	I <sub>OH</sub> = 400 μA		V <sub>CC</sub> -2			٧
VOL	Low Level Output Voltage	V <sub>CC</sub> = 4.5V	54ALS/74ALS IOL = 12mA	Denti he k	.25	.40	V
			74ALS I <sub>OL</sub> = 24mA		.35	.50	V
lį	Input Current at Max Input Voltage	$V_{CC} = 5.5V, V_{IN} = 7V$				100	μΑ
ΙΗ	High Level Input Current	$V_{CC} = 5.5V, V_{IN} = 2.7V$				20	μΑ
IIL	Low Level Input Current	$V_{CC} = 5.5V, V_{IN}$	= 0.4V			-200	μΑ
10	Output Drive Current	V <sub>CC</sub> = 5.5V, V <sub>OL</sub>	JT = 2.25V	-30		-110	mA
lozh	Off-State Output Current, High Bias	V <sub>CC</sub> = 5.5V, V <sub>OL</sub>	JT = 2.7V			20	μΑ
lozL	Off-State Output Current, Low Bias	V <sub>CC</sub> = 5.5V, V <sub>OUT</sub> = 0.4V				-20	μΑ
Icc	Supply Current	V <sub>CC</sub> = 5.5V Data Inputs = 3.0 Select Inputs = 3 Control Inputs = 3	.0V		7.5	12	mA

		2		DM54ALS251			DM74ALS251					
Parameter	From	То	Conditions	Min	Тур	Max	Min	Тур	Max	Unit		
tpLH, Low to high Level Output					7.5			7.5		ns		
tpHL, High to low Level Output		Υ			10.5			10.5		ns		
tpLH, Low to high Level Output	Select	W			10.5			10.5		ns		
tpHL, High to low Level Output		VV			9.5			9.5		ns		
tpLH, Low to high Level Output		Y			4.0			4.0		ns		
tpHL, High to low Level Output	Dete		V <sub>CC</sub> = 4.5 to 5.5V		6.0			6.0		ns		
tpLH, Low to high Level Output	Data	14/	$C_L = 50 \text{ pF}$ $R_1 = 500 \Omega$		6.0			6.0		ns		
tPHL, High to low Level Output		W	HL - 500 12		6.0			6.0		ns		
t <sub>ZH</sub> , Output Enable Time to High Level		Y W Output			4.0			4.0		ns		
t <sub>ZL</sub> , Output Enable Time to Low Level						5.0			5.0		ns	
t <sub>ZH</sub> , Output Enable Time to High Level					4.0			4.0		ns		
t <sub>ZL</sub> , Output Enable Time to Low Level			W	W	W			5.0			5.0	
t <sub>HZ</sub> , Output Disable Time From High Level	Control				3.5			3.5		ns		
t <sub>LZ</sub> , Output Disable Time From Low Level		Y			5.0			5.0		ns		
t <sub>HZ</sub> , Output Disable Time From High Level		W			3.5			3.5		ns		
t <sub>LZ</sub> , Output Disable Time From Low Level					5.0			5.0		ns		

NOTE 1: See notes pg. 1-iii, figures pg. 3-2.

## **Logic Diagram**





## DM54ALS253/DM74ALS253 TRI-STATE® Dual 4-Line to 1-Line Data Selector/Multiplexer

#### **General Description**

This Data Selector/Multiplexer contains full on-chip decoding to select one-of-four data sources as a result of a unique two-bit binary code at the Select Inputs. Each of the two Data Selector/Multiplexer circuits have their own separate Select, Data, and Output Control inputs and a non-inverting Tri-state output buffer. The Output Control inputs, when at the high level, place the corresponding output in the high impedance Off state. In order to prevent bus access conflicts, output disable times are shorter than output enable times. The Select input buffers incorporate internal overlap features to ensure that select input changes do not cause invalid output transients.

#### **Features**

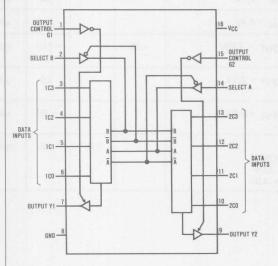
- Advanced Oxide-Isolated Ion-Implanted Schottky TTL Process.
- Switching Performance is Guaranteed Over Full Temperature and V<sub>CC</sub> Supply Range.

- Pin and Functional Compatible with LS Family Counterpart.
- Improved Output Transient Handling Capability.
- Output Control Circuitry Incorporates Power-Up Tri-State Feature.

#### **Absolute Maximum Ratings**

Supply Voltage, VCC	7.0V
Input Voltage	7.0V
Operating Free Air Temperature R	ange
DM54ALS253	-55°C to 125°C
DM74ALS253	0° to 70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature	
(Soldering, 10 seconds)	+300°C

## **Connection Diagram**



#### 54ALS253 (J) 74ALS253 (J,N)

#### **Function Table**

	ect		Data Inputs			Output Control	Output
В	Α	CO	C1	C2	C3	G	Y
X	X	X	X	X	X	Н	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	Н
L	Н	X	L	X	X	L	L
L	Н	X	Н	X	X	L	Н
Н	L	X	X	L	X	L	L
Н	L	X	X	Н	X	L	Н
H	Н	X	X	X	L	L	L
Н	H	X	X	X	Н	L	Н

Address inputs A and B are common to both sections H = High Level, L = Low Level, X = Don't Care, Z = High Impedance

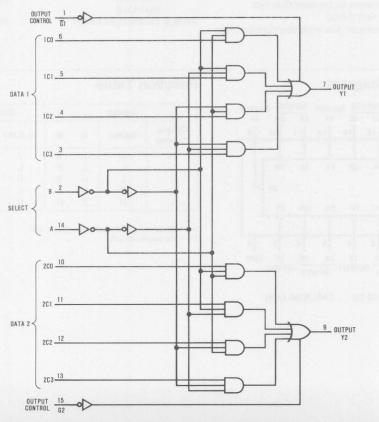
	D	M54ALS2	D	53			
Parameter	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, VCC	4.5	5	5.5	4.5	5	5.5	٧
High Level Input Voltage, VIH	2		Rapit	2	RIF.	81.1	٧
Low Level Input Voltage, VIL	nuesia englasi dera		0.8			0.8	٧
High Level Output Current, IOH			-1.0		eig alle	-2.6	mA
Low Level Output Current, IOL			12			24	mA

	Parameter	Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Voltage	V <sub>CC</sub> = 4.5V, I <sub>IN</sub>	= -18mA			-1.5	V
Vон	High Level Output	$V_{CC} = 4.5V$ , $I_{OH}$	= Max	2.4	3.2	B.7,41	٧
	Voltage	$I_{OH}=400~\mu A$		V <sub>CC</sub> -2			٧
VOL	Low Level Output Voltage	V <sub>CC</sub> = 4.5V	54/74ALS I <sub>OL</sub> = 12mA	intered spec	.25	.40	٧
			74ALS IOL = 24mA		.35	.50	٧
IĮ	Input Current at Max Input Voltage	V <sub>CC</sub> = 5.5V, V <sub>IN</sub> = 7V				100	μΑ
IIH	High Level Input Current	$V_{CC} = 5.5V, V_{IN} = 2.7V$		THE RES	Titles Fill	20	μΑ
IIL	Low Level Input Current	$V_{CC} = 5.5V, V_{IN}$	= 0.4V		- Indian	-200	μΑ
10	Output Drive Current	V <sub>CC</sub> = 5.5V, V <sub>OL</sub>	JT = 2.25V	-30		-110	mA
lozh	Off-State Output Current, High Bias	$V_{CC} = 5.5V, v_{OU}$	TT = 2.7V			20	μΑ
lozL	Off-State Output Current, Low Bias	V <sub>CC</sub> = 5.5V, V <sub>OUT</sub> = 0.4V				-20	μΑ
Icc	Supply Current	V <sub>CC</sub> = 5.5V Data Inputs = 3.0V Select Inputs = 3.0V Control Inputs = 3.0V			7.6	12	mA

				DN	154ALS	253	DM74ALS253			1114
Parameter	From	То	Conditions	Min	Тур	Max	Min	Тур	Max	Unit
tpLH, Low to high Level Output	660 1	Ta.	R-AT		7.5			7.5		ns
tpHL, High to low Level Output	Select			STE S	9.0		nei	9.0		ns
tpLH, Low to high Level Output		P Data	V <sub>CC</sub> =		4.0			4.0		ns
tPHL, High to low Level Output	Data				6.0			6.0		ns
t <sub>ZH</sub> , Output Enable Time to High Level			4.5 to 5.5V $C_L = 50 \text{ pF}$ $R_L = 500 \Omega$	E numb	4.0	Andreas Ministery		4.0		ns
t <sub>ZL</sub> , Output Enable Time to Low Level	Output	Y			5.0	energiale energiale		5.0		ns
t <sub>HZ</sub> , Output Disable Time From High Level	Control		Complete March		4.0			4.0		ns
t <sub>LZ</sub> , Output Disable Time From Low Level	n sminni		lossia i		5.0	(art au		5.0		ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-2.

## **Logic Diagram**



Preliminary



# DM54ALS/DM74ALS257,258 TRI-STATE® Quad 2-Data Selectors/Multiplexers

#### **General Description**

These data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four TRI-STATE outputs that can interface directly with data lines of bus-organized systems. A 4-bit word selected from one of two sources is routed to the four outputs. The ALS257 presents true data whereas the ALS258 presents inverted data to minimize propagation delay time.

This TRI-STATE output feature means that n-bit (paralleled) data selectors with up to 258 sources can be implemented for data buses. It also permits the use of standard TTL registers for data retention throughout the system.

#### **Features**

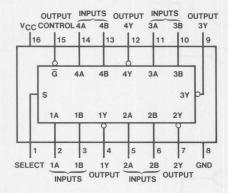
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.

- Functionally and Pin for Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.
- 3-State Buffer-Type Outputs Drive Bus Lines Directly.
- Expand any data input point.
- Multiplex dual data buses.
- General four functions of two variables (one variable is common).
- Source programmable counters.

## **Absolute Maximum Ratings**

Supply Voltage 7V
Input Voltage 7V
Operating Free Air Temperature Range
DM54ALS -55°C to 125°C
DM74ALS 0°C to 70°C
Storage Temperature Range -65°C to 150°C

## **Connection Diagram**



54ALS258 (J) 74ALS258 (J,N)

#### **Function Table**

	Inputs		Output Y				
Output Control	Select	A	В	ALS257	ALS258		
Н	X	X	X	Z	Z		
L	L	L	X	L	Н		
L	L	Н	X	Н	L		
L	Н	X	L	L	Н		
L	Н	X	Н	Н	L		

H = High Level, L = Low Level, X = Don't Care

Z = High Impedance (off)

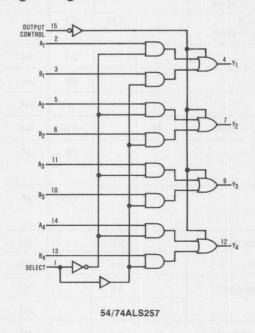
DM	54ALS257	,258	DM	,258		
Min	Nom	Max	Min	Nom	Max	Unit
4.5	5	5.5	4.5	5	5.5	V
		5.5			5.5	V
2			2	T. Und	Oleven -	V
		0.8			0.8	٧
	Tell S	-1.0			-2.6	mA
Va Turner		12	THE T		24	mA
	Min 4.5	Min Nom 4.5 5	4.5 5 5.5 5.5 2 0.8 -1.0	Min         Nom         Max         Min           4.5         5         5.5         4.5           5.5         2         2           0.8         -1.0	Min         Nom         Max         Min         Nom           4.5         5         5.5         4.5         5           5.5         2         2         2           0.8         -1.0         -1.0         -1.0	Min         Nom         Max         Min         Nom         Max           4.5         5         5.5         5.5           5.5         5.5         5.5           2         2         0.8           -1.0         -2.6

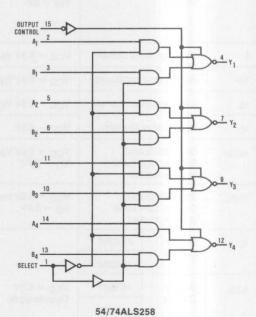
	Parameter		Conditions		Min	Тур	Max	Unit
VIK	Input Clamp	Voltage	V <sub>CC</sub> = 4.5V I <sub>I</sub> =	-18mA			-1.5	V
Vон	High Level Voltage	Output	V <sub>CC</sub> = 4.5V V <sub>IL</sub> = V <sub>IL</sub> MAX	54/74ALS IOH = -1mA	2.4	3.2	19=0.57	V
			601 188	$74ALS$ $I_{OH} = -2.6mA$	2.4	3.3		V
			$I_{OH} = -400\mu A$	54/74ALS	V <sub>CC</sub> -2		THE PLAN	V
VOL	Low Level	Output	$V_{CC} = 4.5V$ $V_{IH} = 2V$	54/74ALS I <sub>OL</sub> = 12mA		0.25	0.4	V
			1 Toron	74ALS I <sub>OL</sub> = 24mA		0.35	0.5	V
lj .	Max High I	nput Current	V <sub>CC</sub> = 5.5V V <sub>IH</sub> =	= 7V			0.1	mA
liH	High Level	Input Current	$V_{CC} = 5.5V V_{IH} =$	= 2.7V	HOL		20	μΑ
IIL	Low Level	Input Current	$V_{CC} = 5.5 V V_{IL} =$	= 0.4V			-0.2	mA
10	Output Driv	e Current	$V_{CC} = 5.5V$	V <sub>O</sub> = 2.25V	-30		-110	mA
lozh	Off-State C Current, Hi Voltage Ap	gh Level	$V_{CC} = 5.5V V_{IH} = V_{O} = 2.7V$	= 2V			20	μΑ
lozL	Off-State C Current, Lo Voltage Ap	w Level	$V_{CC} = 5.5V V_{IH} = 0.4V$	= 2V	19		-20	μА
ІССН	Supply	ALS257		Outputs High		2.6		mA
	Current	ALS258	September 1		HILL	2.4		mA
ICCL	Supply	ALS257	V <sub>CC</sub> = 5.5V	Outputs Low		8.0		mA
	Current	ALS258	Outputs Open		No. 100	7.0		mA
ICCZ	Supply	ALS257		Outputs Disabled		9.3		mA
	Current	ALS258				8.0		mA

Parameter					DM5	4ALS25	7,258	DM74ALS257,258			I I mit
		From	То	Conditions	Min	Тур	Max	Min	Тур	Max	Unit
T <sub>PLH</sub> , Propagation Delay Time.	257	e sale	1 B B B B B B B B B B B B B B B B B B B		1.7	3.5	8.7	1.7	3.5	7.0	4000
Low to high Level Output	258	Data	Any		1.7	3.5	8.7	1.7	3.5	7.0	
T <sub>PHL</sub> , Propagation Delay Time.	257	Data	Y		2.5	5.0	12.5	2.5	5.0	10.0	
High to low Level Output	258			2.5	5.0	12.5	2.5	5.0	10.0	l-nath	
T <sub>PLH</sub> , Propagation Delay Time.	257				3.2	6.5	16.2	3.2	6.5	13.0	-
Low to high Level Output	258	Select	Any Y	V <sub>CC</sub> =	2.7	5.5	13.7	2.7	5.5	11.0	ns
T <sub>PHL</sub> , Propagation Delay Time. High to low Level Output	257				3.5	7.0	17.5	3.5	7.0	14.0	
	258			$4.5 \text{ to } 5.5 \text{V}$ $C_1 = 50 \text{ pF}$	4.0	8.0	20.0	4.0	8.0	16.0	
TZH, Output Enable Time to	257	Output	Δην	$\begin{array}{c} R_L = 500 \Omega \\ \text{Any} \\ \text{Y} \end{array}$	2.0	4.0	10.0	2.0	4.0	8.0	
High Level	258				2.0	4.0	10.0	2.0	4.0	8.0	
TZL, Output Enable Time to	257	Control	,		2.5	5.0	12.5	2.5	5.0	10.0	
Low Level	258				2.5	5.0	12.5	2.5	5.0	10.0	
T <sub>HZ</sub> , Output Disable Time.	257				2.5	5.0	12.5	2.5	5.0	10.0	
From High Level	258	Output	Any		2.5	5.0	12.5	2.5	5.0	10.0	
T <sub>LZ</sub> , Output Disable Time	257	Control	Y		5.0	10.0	25.0	5.0	10.0	20.0	
From Low Level	258				5.0	10.0	25.0	5.0	10.0	20.0	

NOTE 1: See notes pg. 1-iii, figures pg. 3-2.

## **Logic Diagrams**







# DM54ALS273/DM74ALS273 Octal D-Type Edge-Triggered Flip-Flops With Clear

## **General Description**

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic with a direct clear input. The outputs are buffer type and are, thus, guaranteed at  $I_{OL}$  12/24 mA.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

#### **Features**

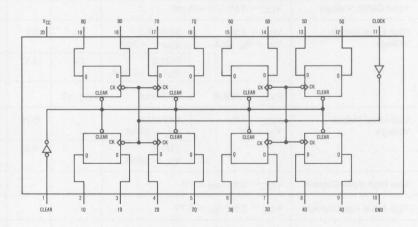
Switching Specifications at 50 pF.

- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Buffer-Type Outputs and Improved AC Offer Significant Advantage Over 'LS273.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process
- Functionally and Pin-For-Pin Compatible with 'LS273.

#### **Absolute Maximum Ratings**

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS273	-55°C to 125°C
DM74ALS273	0°C to 70°C
Storage Temperature Range	-65°C to 150°C

## **Connection Diagram**



54ALS273 (J) 74ALS273 (J,N)

		D	M54ALS2	73	D			
Parameter		Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, VCC		4.5	5	5.5	4.5	5	5.5	٧
High Level Input Voltage, VIH		2			2			V
Low Level Input Voltage, VIL				0.8	i de la constante de la consta		0.8	V
High Level Output Current, IOH				-1.0			-2.6	mA
Low Level Output Current, IOL				12	Hug m		24	mA
Clock frequency, fCLOCK		0		30	0		35	MHz
Width of Clock Pulse, Tw	High	10			10			ns
PLEASURE PROFILE	Low	17			15			ns
Width of Clear Pulse, TW	Low	10			10			ns
Data Setup Time, T <sub>SU</sub>		10↑			10↑			ns
Data Hold Time, T <sub>H</sub>		41			01		F- + 1	ns

The (1) arrow indicates the positive edge of the Clock is used for reference.

	Parameter	Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Voltage	V <sub>CC</sub> = 4.5V I <sub>I</sub> = -	18 mA			—1.5	V
VOH	High Level Output Voltage	$V_{CC} = 4.5V$ $V_{IL} = V_{IL} MAX$	54/74ALS I <sub>OH</sub> = -1mA	2.4	3.2		٧
			$74ALS$ $I_{OH} = -2.6mA$	2.4	3.3		V
		$I_{OH} = -400\mu A$	54/74ALS	V <sub>CC</sub> -2			٧
VOL	Low Level Output Voltage	V <sub>CC</sub> = 4.5V V <sub>IH</sub> = 2V	54/74ALS I <sub>OL</sub> = 12mA		0.25	0.4	V
			74ALS I <sub>OL</sub> = 24mA		0.35	0.5	V
lį .	Max High Input Current	V <sub>CC</sub> = 5.5V V <sub>IH</sub> =	7V			0.1	mA
ΊΗ	High Level Input Current	V <sub>CC</sub> = 5.5V V <sub>IH</sub> =	2.7V			20	μΑ
IIL	Low Level Input Current	V <sub>CC</sub> = 5.5V V <sub>IL</sub> =	0.4V			-0.2	mA
10	Output Drive Current	V <sub>CC</sub> = 5.5V	54/74ALS V <sub>O</sub> = 2.25V	-30		-110	mA
Icc	Supply Current	V <sub>CC</sub> = 5.5V	Outputs High		11	18	mA
		Outputs Open	Outputs Low		19	29	mA

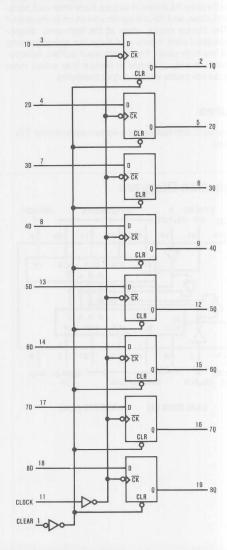
			DM54ALS273			D				
Parameter	From	То	Conditions	Min	Тур	Max	Min	Тур	Max	Unit
FMAX			$V_{CC} = 4.5V \text{ to } 5.5V$	30			35			MHz
TPHL	Clear	Any Q	$R_L = 500 \Omega$ $C_L = 50 \text{ pF}.$	7		24	7		21	ns
TPLH	Clock	Any Q	00 pr.	4		15	4	ii.	12	ns
TPHL	J.00K	, iiiy G		4		15	4		12	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-3.

#### **Function Table** (Each Flip-Flop)

	Inputs		Output
Clear	Clock	D	Q
L	X	X	L
Н	1	Н	Н
Н	1	L	L
Н	L	X	Qn

## **Logic Diagram**



L = Low State, H = High State, X = Don't Care† = Positive Edge Transition,  $Q_0 = Previous Condition of Q$ 

## DM54ALS352/DM74ALS352 Dual 4-Line to 1-Line Data Selector/Multiplexer

## **General Description**

This Data Selector/Multiplexer contains full on-chip decoding to select one-of-four data sources as a result of a unique two-bit binary code at the Select inputs. Each of the two Data Selector/Multiplexer circuits have their own separate Select, Data, and Strobe inputs and an inverting output buffer. The Strobe inputs, when at the high level, disable their associated data inputs and force the corresponding output to the high state. The Select input buffers incorporate internal overlap features to ensure that select input changes do not cause invalid output transients.

#### **Features**

Advanced Oxide-isolated Ion-implanted Schottky TTL process.

- Switching performance is guaranteed over full temperature and V<sub>CC</sub> supply range.
- Pin and functional compatible with the LS Family counterpart.
- Improved output transient handling capability.

## **Absolute Maximum Ratings**

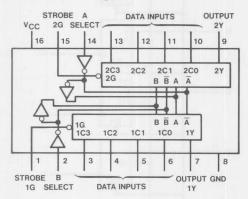
Supply Voltage 7.0V
Input Voltage 7.0V
Operating Free Air Temperature Range
DM54ALS352 -55°C to 125°C

DM54ALS352 -55°C to 125°C
DM74ALS352 0°C to 70°C
Storage Temperature Range -65°C to 150°C
Lead Temperature

(Soldering, 10 seconds)

+300°C

## **Connection Diagram**



54ALS352 (J) 74ALS352 (J,N)

#### **Function Table**

Select Inputs			Data	Inputs	Strobe	Output	
В	Α	CO	C1	C2	C3	G	Υ
Χ	X	X	Х	Х	Х	Н	Н
L	L	L	X	X	X	L	Н
L	L	Н	X	X	X	L	L
L	Н	X	L	X	X	L	H
L	Н	X	Н	X	X	L	L
Н	L	X	X	L	X	L	Н
Н	L	X	X	Н	X	L	L
Н	Н	X	X	X	L	L	Н
Н	Н	X	X	X	Н	L	L

Select inputs A and B are common to both sections  $H = High \ Level, \ L = Low \ Level, \ X = Don't \ Care$ 

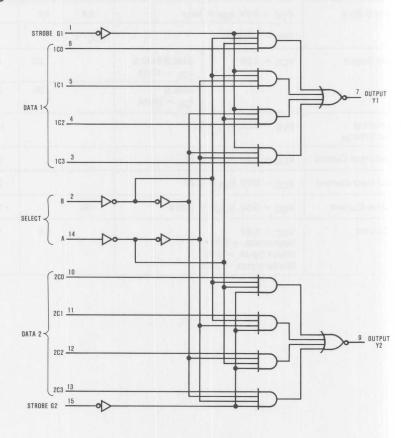
	D	M54ALS3	52	D	52		
Parameter	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, VCC	4.5		5.5	4.5	la Calleria	5.5	V
High Level Input Voltage, VIH	2.0		Tellal .	2.0	EQ Pre		٧
Low Level Input Voltage, VIL			0.8		ge Ci Ismal	0.8	V
High Level Output Current, IOH	1 -466.4		-1.0	l h	100 918	-2.6	mA
Low Level Output Current, IOL			12		let incl	24	mA

	Parameter	Conditions		Min	Тур	Max	Uni
VIK	Input Clamp Voltage	$V_{CC} = 4.5V, I_{IN}$	= -18mA			-1.5	٧
VOH	High Level Output	$V_{CC} = 4.5V, I_{OH}$	= Max	2.4	3.2		V
	Voltage	$IOH = -400\mu A$		V <sub>CC</sub> -2			V
VOL	Low Level Output Voltage	V <sub>CC</sub> = 4.5V	54ALS/74ALS i <sub>OL</sub> = 12mA		.25	.40	V
			74ALS I <sub>OL</sub> = 24mA		.35	.50	V
lį	Input Current at Max Input Voltage	V <sub>CC</sub> = 5.5V, V <sub>IN</sub> = 7V				100	μΑ
lін	High Level Input Current	$V_{CC} = 5.5V, V_{IN}$	= 2.7V			20	μΑ
IIL	Low Level Input Current	$V_{CC} = 5.5V, V_{IN}$	= 0.4V			-200	μΑ
IO	Output Drive Current	$V_{CC} = 5.5V, V_{OU}$	JT = 2.25V	-30		-110	mA
ICC	Supply Current	V <sub>CC</sub> = 5.5V Date Inputs = 3.0 Select Inputs = 3 Strobe Inputs = 0	.0V	4	6.5	10	mA

				DM54ALS352			DM74ALS352			Unit
Parameter	From	То	Conditions	Min	Тур	Max	Min	Тур	Max	Unit
tPLH, Low to high Level Output					9.0			9.0		ns
tpHL, High to low Level Output	Select				9.5			9.5		ns
tpLH, Low to high Level Output		Υ	$V_{CC} = 4.5 \text{ to } 5.5 \text{V}$ $C_L = 50 \text{ pF}$ $R_L = 500 \Omega$		6.0			6.0		ns
tpHL, High to low Level Output	Data				6.0			6.0		ns
tPLH, Low to high Level Output	04				4.0		i Pinn	4.0	17972	ns
tpHL, High to low Level Output	Strobe				5.0			5.0		ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-1.

## **Logic Diagram**





## DM54ALS353/DM74ALS353 TRI-STATE® Dual 4-Line to 1-Line Data Selector/Multiplexer

#### **General Description**

This Data Selector/Multiplexer contains full on-chip decoding to select one-of-four data sources as a result of a unique two-bit binary code at the Select inputs. Each of the two Data Selector/Multiplexer circuits have their own separate Select, Data, and Output Control inputs and an inverting TRI-STATE output buffer. The Output Control inputs, when at the high level, place the corresponding output in the high impedance Off state. In order to prevent bus access conflicts, output disable times are shorter than output enable times. The Select input buffers incorporate internal overlap features to ensure that select input changes do not cause invalid output transients.

#### **Features**

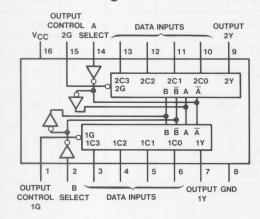
- Advanced Oxide-isolated Ion-implanted Schottky TTL process.
- Switching performance is guaranteed over full temperature and V<sub>CC</sub> supply range.

- Pin and functional compatible with LS Family counterpart.
- Improved output transient handling capability.
- Output Control circuitry incorporates power-up TRI-STATE feature.

#### **Absolute Maximum Ratings**

Supply Voltage	7.0V
Input Voltage	7.0V
Operating Free Air Temperature R	ange
DM54ALS353	-55°C to +125°C
DM74ALS353	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature	
(Soldering, 10 seconds)	+300°C

#### **Connection Diagram**



54ALS353 (J) 74ALS353 (J,N)

#### **Function Table**

	ect uts		Data	Inputs		Output Control	Output
В	Α	CO	C1	C2	C3	G	Υ
Χ	X	X	X	X	X	Н	Z
L	L	L	X	X	X	L	Н
L	L	Н	X	X	X	L	L
L	Н	X	L	X	X	L	Н
L	Н	X	Н	X	X	L	L
Н	L	X	X	L	X	L	Н
Н	L	X	X	Н	X	L	L
H	Н	X	X	X	L	L	Н
Н	Н	X	X	X	Н	L	L

Address inputs A and B are common to both sections H = High Level. L = Low Level. X = Don't Care.

Z = High Impedance State

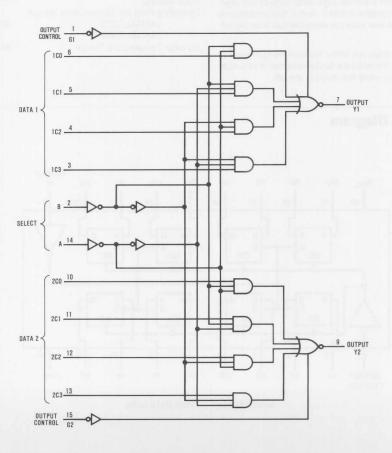
	DM54ALS353			DM74ALS353			
Parameter	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, V <sub>CC</sub>	4.5	9681	5.5	4.5		5.5	V
High Level Input Voltage, VIH	2.0		1011	2.0	ale i		٧
Low Level Input Voltage, VIL	Alima nazi siya sadi.		0.8	unital Cri		0.8	٧
High Level Output Current, IOH			-1.0			-2.6	mA
Low Level Output Current, IOL	1000 6 123	Marine 1 of	12	TIMES TO		24	mA

	Parameter	Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Voltage	$V_{CC} = 4.5V$ , $I_{IN} = -18$ mA				-1.5	V
Vон	High Level Output	$V_{CC} = 4.5V$ , $I_{OH} = Max$		2.4	3.2	201	V
	Voltage	$IOH = -400\mu A$		V <sub>CC</sub> -2			٧
VOL	Low Level Output Voltage	V <sub>CC</sub> = 4.5V	54ALS/74ALS I <sub>OL</sub> = 12mA	daires berd	.25	.40	V
			74ALS I <sub>OL</sub> = 24mA	Traing III 854	.35	.50	V
lį	Input Current at Max Input Voltage	$V_{CC} = 5.5V, V_{IN} = 7V$				100	μΑ
ΊΗ	High Level Input Current	$V_{CC} = 5.5V, V_{IN} = 2.7V$		Minister		20	μΑ
I <sub>I</sub> L	Low Level Input Current	$V_{CC} = 5.5V, V_{IN}$	= 0.4V	ana	A LITTLE	-200	μΑ
IO	Output Drive Current	$V_{CC} = 5.5V, V_{OU}$	JT = 2.25V	-30		-110	mA
lozh	Off-State Output Current, High Bias	$V_{CC} = 5.5V, V_{OU}$	<sub>JT</sub> = 2.7V			20	μΑ
lozL	Off-State Output Current, Low Bias	$V_{CC} = 5.5V, V_{OU}$	JT = 0.4V			-20	μΑ
Icc	Supply Current	V <sub>CC</sub> = 5.5V Date Inputs = 3.0 Select Inputs = 3 Control Inputs =	3.0V		8.0	12	mA

#### Switching Characteristics over recommended operating free air temperature range (Note 1) DM54ALS353 DM74ALS353 Unit Parameter From To Conditions Max Тур Max Min Тур 9.0 9.0 tpLH, Low to high Level Output ns Select tpHL, High to low Level Output 9.5 9.5 ns 6.0 6.0 tpLH, Low to high Level Output ns Data tpHL, High to low Level Output 6.0 6.0 ns V<sub>CC</sub> = 4.5 to 5.5V Υ tzH, Output Enable Time 4.0 4.0 ns $\begin{array}{l} \text{C}_{\text{L}} = 50 \; \text{pF} \\ \text{R}_{\text{L}} = 500 \; \Omega \end{array}$ to High Level tzL, Output Enable Time 5.0 5.0 ns to Low Level Output Control tHZ, Output Disable Time 4.0 4.0 ns From High Level tLZ, Output Disable Time 5.0 5.0 ns From Low Level

NOTE 1: See notes pg. 1-iii, figures pg. 3-2.

## **Logic Diagram**



# DM54ALS373/DM74ALS373 Octal D-Type Transparent Latches

## **General Description**

These 8-bit registers feature totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the ALS373 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was set up.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches. That is, the old data can be retained or new data can be entered even while the outputs are off.

#### **Features**

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with LS TTL Counterpart.
- Improved AC Performance Over LS373 at Approximately Half the Power.
- 3-State Buffer-Type Outputs Drive Bus Lines Directly.

## **Absolute Maximum Ratings**

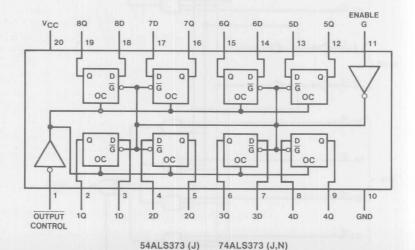
Supply Voltage
Input Voltage
Operating Free Air Temperature Range
DM54ALS373
DM74ALS373

Storage Temperature Range

-55°C to 125°C 0°C to 70°C -65°C to 150°C

7V

**Connection Diagram** 



	D	M54ALS3	73	D	M74ALS3	73	
Parameter	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, VCC	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, VIH	2			2			V
Low Level Input Voltage, VIL			0.8			0.8	V
High Level Output Voltage, VOH			5.5			5.5	V
High Level Output Current, IOH			-1.0	i i gr		-2.6	mA
Low Level Output Current, IOL			12			24	mA
Width of Enable Pulse, High or Low	10			10			ns
Data Setup Time, TSU	10↓			10↓			ns
Data Hold Time, T <sub>H</sub>	7↓			7↓			ns

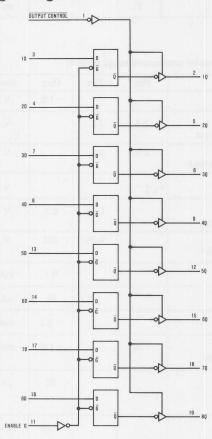
The (1) arrow indicates the negative edge of the enable is used for reference.

	Parameter	Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Voltage	V <sub>CC</sub> = 4.5V I <sub>I</sub> =	-18mA			-1.5	V
Vон	High Level Output Voltage	V <sub>CC</sub> = 4.5V V <sub>IL</sub> = V <sub>IL</sub> MAX	54/74ALS I <sub>OH</sub> = -1mA	2.4	3.2		V
			74ALS I <sub>OH</sub> = -2.6mA	2.4	3.3		V
		$I_{OH} = -400\mu A$	54/74ALS	V <sub>CC</sub> -2			V
VOL	Low Level Output Voltage	V <sub>CC</sub> = 4.5V V <sub>IH</sub> = 2V	54/74ALS I <sub>OL</sub> = 12mA		0.25	0.4	٧
			74ALS I <sub>OL</sub> = 24mA		0.35	0.5	V
lį	Max High Input Current	$V_{CC} = 5.5V V_{IH} = 7V$				0.1	mA
ΙΗ	High Level Input Current	$V_{CC} = 5.5V V_{IH} = 2.7V$				20	μΑ
IIL	Low Level Input Current	$V_{CC} = 5.5 V V_{IL} =$	= 0.4V			-0.2	mA
10	Output Drive Current	V <sub>CC</sub> = 5.5V	54/74ALS V <sub>O</sub> = 2.25V	-30		-110	mA
lozh	Off-State Output Current, High Level Voltage Applied	$V_{CC} = 5.5V V_{IH} = 0.000 V_{O} = 2.7V$	= 2V			20	μΑ
lozL	Off-State Output Current, Low Level Voltage Applied	$V_{CC} = 5.5V V_{IH} = 0.4V$	= 2V			-20	μΑ
Icc	Supply Current	V <sub>CC</sub> = 5.5V	Outputs High		9	14	mA
		Outputs Open	Outputs Low		16	25	mA
		11 30 1-6	Outputs Disabled		17	27	mA

	I I STATISTICAL			Di	M54ALS	373	DI	VI74ALS	173	Unit
Parameter Fro	From	То	Conditions	Min	Тур	Max	Min	Тур	Max	
TPLH	Data	Any Q	of the second	3		15	3		12	ns
TPHL	Dutu	7.117 &		3		15	3		12	ns
TPLH	Enable	Any Q	$V_{CC} = 4.5V \text{ to } 5.5V$	8		25	8		20	ns
TPHL		, ~	$R_L = 500 \Omega$	8		22	8		20	ns
TPZH			$C_L = 50 \text{ pF}$	3		18	4		15	ns
TPZL	Output	Any Q		4		21	5		18	ns
TPHZ	Control	7, &		2		12	2		10	ns
TPLZ				3		15	3		13	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-5.

## **Logic Diagram**



## **Function Table**

Output Control	Enable G	D	Output Q
L	Н	Н	Н
L	Н	L	L
L	L	X	Qn
Н	X	X	Z

L= Low State, H= High State, X= Don't Care Z= High Impedance State  $Q_0=$  Previous Condition of Q



## DM54ALS374/DM74ALS374 Octal D-Type-Edge-Triggered Flip-Flops

#### **General Description**

These 8-bit registers feature totem-pole three-state output designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the ALS374 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

#### **Features**

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin-for-Pin Compatible with LS TTL Counterpart.
- Improved AC Performance Over LS374 at Approximately Half the Power.
- TRI-STATE® Buffer-Type Outputs Drive Bus Lines Directly.

## **Absolute Maximum Ratings**

 Supply Voltage
 7V

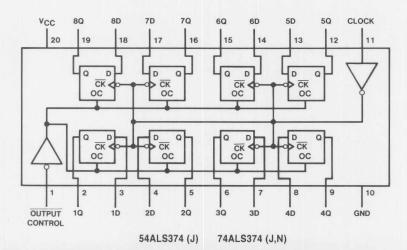
 Input Voltage
 7V

 Operating Free Air Temperature Range
 —55°C to 125°C

 DM74ALS374
 —0°C to 70°C

 Storage Temperature Range
 —65°C to 150°C

## **Connection Diagram**



		D	M54ALS3	74	D	M74ALS37	74	
Parameter		Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, V <sub>CC</sub>		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, VIH		2	imig	9-9/19	2	regh		V
Low Level Input Voltage, VIL				0.8			0.8	V
High Level Output Voltage, VOH				5.5			5.5	V
High Level Output Current, IOH				-1.0	points	M MEN	-2.6	mA
Low Level Output Current, IOL	mi-sunist? basi jaji			12	wildigensi- wildigensi-		24	mA
Clock frequency, fCLOCK	MARKEN	0		30	0	reside of co	35	МН
Width of Clock Pulse, Tw	High	10			10	instruction in		ns
Low		17			15	I la rise		ns
Data Setup Time, T <sub>SU</sub>		10↑			10↑			ns
Data Hold Time, T <sub>H</sub>		41	Course Lat		01			ns

The (1) arrow indicates the positive edge of the Clock is used for reference.

	Parameter	Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Voltage	V <sub>CC</sub> = 4.5V I <sub>I</sub> =	-18mA			-1.5	V
Vон	High Level Output Voltage	$V_{CC} = 4.5V$ $V_{IL} = V_{IL} MAX$	54/74ALS I <sub>OH</sub> = -1mA	2.4	3.2		٧
			74ALS I <sub>OH</sub> = -2.6mA	2.4	3.3		V
		$I_{OH} = -400\mu A$	54/74ALS	V <sub>CC</sub> -2			V
VOL	Low Level Output Voltage	V <sub>CC</sub> = 4.5V V <sub>IH</sub> = 2V	54/74ALS I <sub>OL</sub> = 12mA		0.25	0.4	V
			74ALS I <sub>OL</sub> = 24mA		0.35	0.5	V
lį –	Max High Input Current	$V_{CC} = 5.5V V_{IH}$	= 7V			0.1	mA
ΙΗ	High Level Input Current	$V_{CC} = 5.5V V_{IH}$	= 2.7V			20	μΑ
IIL	Low Level Input Current	$V_{CC} = 5.5 \text{V V}_{IL} =$	= 0.4V			-0.2	mA
10	Output Drive Current	$V_{CC} = 5.5V$	54/74ALS V <sub>O</sub> = 2.25V	-30		-110	mA
lozh	Off-State Output Current, High Level Voltage Applied	$V_{CC} = 5.5V V_{IH}$ $V_{O} = 2.7V$	= 2V			20	μΑ
IOZL	Off-State Output Current, Low Level	$V_{CC} = 5.5V V_{IH}$ $V_{O} = 0.4V$	= 2V			-20	μΑ

V<sub>CC</sub> = 5.5V Outputs Open

			Conditions	Di	M54ALS3	374	DI	M74ALS3	374	
Parameter	From	То		Min	Тур	Max	Min	Тур	Max	Unit
FMAX				30			35			MHz
TPLH	Clock	Any Q		4		15	4		12	ns
TPHL		7.11.7 =		4		15	4		12	ns
T <sub>PZH</sub>	Output	Any Q	$V_{CC} = 4.5V \text{ to } 5.5V$ $R_L = 500 \Omega$	3		18	4		15	ns
TPZL	Control	7,	C <sub>L</sub> = 50 pF	4		21	5	Mi.	18	ns
T <sub>PHZ</sub>				2		12	2		10	ns
TPLZ				2		15	3		13	ns

Outputs High

Outputs Low

Outputs Disabled

11

19

20

17

28

31

mA

mA

mA

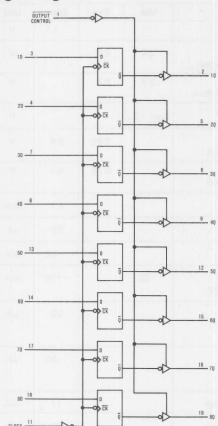
NOTE 1: See notes pg. 1-iii, figures pg. 3-5.

Voltage Applied

Supply Current

ICC

## **Logic Diagram**



## **Function Table**

Output Control	Clock	D	Output
L	1	Н	Н
L	1	L	L
L	L	X	Q <sub>0</sub>
Н	X	X	Z

L = Low State, H = High State, X = Don't Care

↑ = Positive Edge Transition

Z = High Impedance State

Q<sub>0</sub> = Previous Condition of Q



## DM54ALS/DM74ALS518,519,520,521,522 8-Bit Comparators

#### **General Description**

These comparators perform an "equal to" comparison of two eight-bit words with provision for expansion or external enabling. The matching of the two 8-bit input plus a logic LOW on the  $\overline{\text{EN}}$  input produces the output A=B on the ALS518 & 519 and the output  $\overline{A}=\overline{B}$  on the ALS520, 521 & 522. The ALS520 & 521 have totem pole outputs, while the ALS518, 519 & 522 have open collector outputs for wire AND cascading. Additionally, the ALS518, 520 & 522 are provided with B input pull up termination resistors for analog or switch data.

#### **Features**

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.

- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin for Pin Compatible with LS Family Counterpart.
- Improved Output Transient Handling Capability.

### **Absolute Maximum Ratings**

 Supply Voltage
 7V

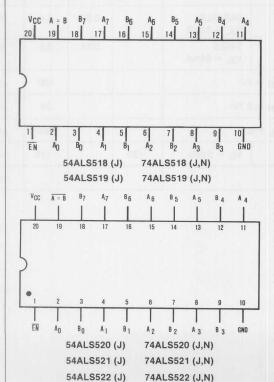
 Input Voltage
 7V

 Operating Free Air Temperature Range
 —55°C to 125°C

 DM74ALS
 —0°C to 70°C

 Storage Temperature Range
 —65°C to 150°C

#### **Connection Diagram**



#### **Function Tables**

#### ALS518,519

	Inputs	Output
EN	Data	A = B
L L	A=B	Н
L	A≠B	L
Н	X	Holl L

H = High Logic Level; L = Low Logic Level; X = Don't Care

## ALS520,521,522

Ing	outs	Output
EN	Data	$\overline{A}=\overline{B}$
L	A=B	L
L	A≠B	Н
Н	X	Н

H = High Logic Level; L = Low Logic Level; X = Don't Care

	518,	518,5	Unit				
Parameter	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, VCC	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, VIH	2			2			V
Low Level Input Voltage, VIL	in a la		0.8	maire	Name C	0.8	V
High Level Output Voltage, VOH (ALS518,519,522)	roed w tor		5.5	raig meta raig ven	sq not-	5.5	V
High Level Output Current, IOH (ALS520,521)			-1.0		THE LOS	-2.6	mA
Low Level Output Current, IOL	OHU L ST		12			24	m.A

	Parameter	Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Voltage	$V_{CC} = 4.5V, I_{I} = -$	-18mA			-1.5	V
VOH	High Level Output	$I_{OH} = -400\mu A$ ALS520,521		V <sub>CC</sub> -2	marrayo.	i ilias	V
	Voltage	IOH = MAX		2.4	3.2		V
ЮН	High Level Output Current	V <sub>CC</sub> = 4.5V V <sub>OH</sub> = 5.5V	ALS518, 519,522	Ring	jiū na	100	μΑ
VOL	Low Level Output Voltage	V <sub>CC</sub> = 4.5V	54/74ALS I <sub>OL</sub> = 12mA		0.25	0.4	٧
	and		74ALS I <sub>OL</sub> = 24mA		0.35	0.5	V
lj .	Max High Input Current	V <sub>CC</sub> = 5.5V, V <sub>IH</sub> =	= 7V			100	μΑ
ІІН	High Level Input Current	V <sub>CC</sub> = 5.5V, V <sub>IH</sub> =	= 2.7V			20	μΑ
Iμ	Low Level Input Current	V <sub>CC</sub> = 5.5V, V <sub>IL</sub> =	= 0.4V			-200	μΑ
lo	Output Drive Current	$V_{CC} = 5.5V$	$V_0 = 2.25V$	-30		-110	mA
Icc	Supply Current	$V_{CC} = 5.5V$	(4.6) 001	moral a	10.5		mA

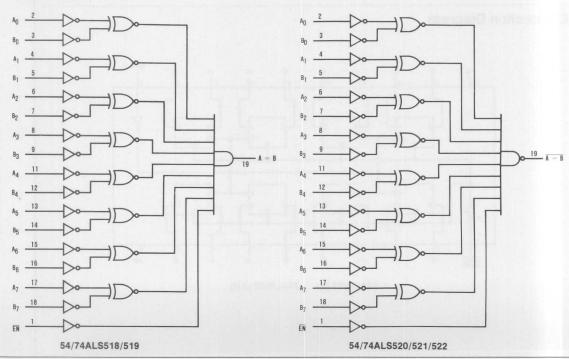
Parameter	From Input	From To		DM54ALS 518,519,522			DM74ALS 518,519,522					
		Output	Conditions	Min	Тур	Max	Min	Тур	Max	Unit		
TPLH, Propagation Delay Time, Low to high Level Output	A or B		VCC = 4.5V to 5.5V	5	15	35	5	15	26			
T <sub>PHL</sub> , Propagation Delay Time, High to low Level Output	Data	A=B or A=B		5	14	33	5	14	27			
TPLH, Propagation Delay Time, Low to high Level Output	ĒN					$C_L = 50pF$ $R_L = 667\Omega$	5	14	33	5	14	24
TPHL, Propagation Delay Time, High to low Level Output		Licencia i		4	12	28	4	12	23			

## Switching Characteristics over recommended operating free air temperature range (Note 1)

mention	From Input	То		DM54ALS 520,521			DM74ALS 520,521							
Parameter		Output	Conditions	Min	Тур	Max	Min	Тур	Max	Unit				
TPLH, Propagation Delay Time, Low to high Level Output	A or B		V <sub>CC</sub> = 4.5V to 5.5V	3	6.5	16	3	6.5	13					
T <sub>PHL</sub> , Propagation Delay Time, High to low Level Output	Data			4	8.5	22	4	8.5	17					
T <sub>PLH</sub> , Propagation Delay Time, Low to high Level Output	A=B	A=B	A=B	A=B	A=B	A=B	$C_L = 50pF$ $R_L = 500\Omega$	3	5.5	14	3	5.5	11	ns
T <sub>PHL</sub> , Propagation Delay Time, High to low Level Output	214			3	6.5	16	3	6.5	13					

NOTE 1: See notes pg. 1-iii, figures pg 3-4 and 3-1.

## **Logic Diagrams**



## DM54ALS533/DM74ALS533 Octal D-Type Transparent Latches With Inverted Outputs

## **General Description**

These 8-bit registers feature totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight inverting latches of the ALS533 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the complement of the data (D) inputs. When the enable is taken low the output will be latched at the complement of the level of the data that was set up.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches. That is, the old data can be retained or new data can be entered even while the outputs are off.

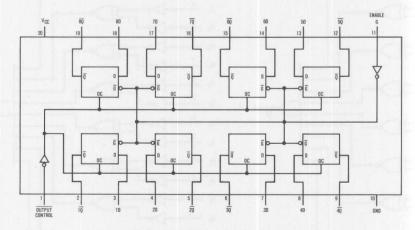
#### **Features**

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced, Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- 3-State Buffer-Type Outputs Drive Bus Lines Directly.

#### **Absolute Maximum Ratings**

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS533	-55°C to 125°C
DM74ALS533	0°C to 70°C
Storage Temperature Range	-65°C to 150°C

## **Connection Diagram**



54ALS533 (J) 74ALS533 (J,N)

	D	M54ALS5	33	D	33	I I m i A	
Parameter	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, VCC	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, VIH	2			2			V
Low Level Input Voltage, VIL			0.8			0.8	V
High Level Output Voltage, VOH			5.5			5.5	V
High Level Output Current, IOH			-1.0		11-70	-2.6	mA
Low Level Output Current, IOL			12			24	mA
Width of Enable Pulse, High or Low	15			15			ns
Data Setup Time, TSU	10↓			10↓		in goal	ns
Data Hold Time, TH	01			01		Mark 1	ns

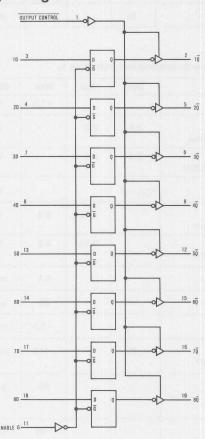
The (1) arrow indicates the negative edge of the enable is used for reference.

	Parameter	Conditions		Min	Тур	Max	Uni
VIK	Input Clamp Voltage	V <sub>CC</sub> = 4.5V I <sub>I</sub> =	-18mA			-1.5	V
VOH	High Level Output Voltage	$V_{CC} = 4.5V$ $V_{IL} = V_{IL} MAX$	54/74ALS I <sub>OH</sub> = -1mA	2.4	3.2		V
			$74ALS$ $I_{OH} = -2.6mA$	2.4	3.3		V
		$I_{OH} = -400\mu A$	54/74ALS	V <sub>CC</sub> -2			V
VOL	Low Level Output Voltage	$V_{CC} = 4.5V$ $V_{IH} = 2V$	54/74ALS I <sub>OL</sub> = 12mA		0.25	0.4	٧
			74ALS I <sub>OL</sub> = 24mA		0.35	0.5	V
lį	Max High Input Current	$V_{CC} = 5.5 V V_{IH}$			0.1	mA	
lін	High Level Input Current	$V_{CC} = 5.5V V_{IH}$	-		20	μΑ	
IIL	Low Level Input Current	V <sub>CC</sub> = 5.5V V <sub>IL</sub> =	V <sub>CC</sub> = 5.5V V <sub>IL</sub> = 0.4V			-0.2	mA
10	Output Drive Current	$V_{CC} = 5.5V$				-110	mA
lozh	Off-State Output Current, High Level Voltage Applied	$V_{CC} = 5.5V V_{IH}$ $V_{O} = 2.7V$	= 2V			20	μΑ
lozL	Off-State Output Current, Low Level Voltage Applied	$V_{CC} = 5.5V V_{IH}$ $V_{O} = 0.4V$	= 2V			-20	μΑ
Icc	Supply Current	V <sub>CC</sub> = 5.5V	Outputs High		10	15	mA
		Outputs Open	Outputs Low		17	26	mA
			Outputs Disabled		18.5	28	mA

	The late		The state of the s	DM54ALS533			Di	33		
Parameter	From	То	Conditions	Min	Тур	Max	Min	Тур	Max	Unit
TPLH	Data	Any Q		3		15	3		12	ns
TPHL	Julia		$V_{CC} = 4.5V \text{ to } 5.5V$ $R_{L} = 500 \Omega$	3	-	15	3		12	ns
TPLH	Enable	Any Q		8		25	8		20	ns
TPHL	2110010			8		22	8		20	ns
TPZH			$C_L = 50 \text{ pF}$	3		18	4		15	ns
TPZL	Output	Any Q		4		21	5		18	ns
TPHZ	Control	Ally Q		2		12	2		10	ns
TPLZ		111		3		15	3		13	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-5.

## **Logic Diagram**



## **Function Table**

Output Control	Enable G	D	Output Q
L	Н	Н	L
L	Н	L	Н
L	L	X	$\overline{Q}_0$
Н	X	X	Z

L = Low state, H = High State, X = Don't Care

Z = High Impedance State

 $\overline{\mathsf{Q}}_0 = \mathsf{Previous} \; \mathsf{Condition} \; \mathsf{of} \; \overline{\mathsf{Q}}$ 

# DM54ALS534/DM74ALS534 Octal D-Type Edge-Triggered Flip-Flops With Inverted Outputs

#### **General Description**

These 8-bit registers feature totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the ALS534 are edge-triggered inverting D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the complement of the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

#### **Features**

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- 3-State Buffer-Type Outputs Drive Bus Lines Directly.

## **Absolute Maximum Ratings**

 Supply Voltage
 7V

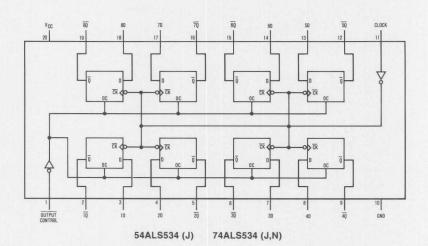
 Input Voltage
 7V

 Operating Free Air Temperature Range
 —55°C to 125°C

 DM54ALS534
 —0°C to 70°C

 Storage Temperature Range
 —65°C to 150°C

## **Connection Diagram**



		0	M54ALS5	34	D	M74ALS5	34	11-74
Parameter		Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, V <sub>CC</sub>		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, VIH		2		T-sp	2			٧
Low Level Input Voltage, VIL				0.8			0.8	V
High Level Output Voltage, VOH				5.5	and the		5.5	V
High Level Output Current, IOH			Lice plan	-1.0			-2.6	mA
Low Level Output Current, IOL	denta			12			24	mA
Clock frequency, fCLOCK	Marketon perform	0		30	0		35	MHz
Width of Clock Pulse, Tw	High	10		nc.an	10			ns
Low		17			15			ns
Data Setup Time, T <sub>SU</sub>		10↑			10↑	FUTUSED A		ns
Data Hold Time, T <sub>H</sub>		4↑			01			ns

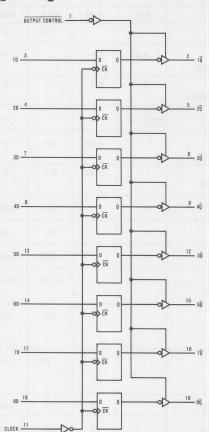
The (1) arrow indicates the positive edge of the Clock is used for reference.

	Parameter	Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Voltage	V <sub>CC</sub> = 4.5V I <sub>I</sub> =	-18mA			-1.5	٧
Vон	High Level Output Voltage	$V_{CC} = 4.5V$ $V_{IL} = V_{IL} MAX$	54/74ALS I <sub>OH</sub> = -1mA	2.4	3.2		V
			$74ALS$ $I_{OH} = -2.6mA$	2.4	3.3		V
		$I_{OH} = -400\mu A$	54/74ALS	V <sub>CC</sub> -2			٧
VOL	Low Level Output Voltage	V <sub>CC</sub> = 4.5V V <sub>IH</sub> = 2V	54/74ALS I <sub>OL</sub> = 12mA		0.25	0.4	V
			74ALS I <sub>OL</sub> = 24mA		0.35	0.5	V
lį	Max High Input Current	$V_{CC} = 5.5V V_{IH} = 7V$				0.1	m/
liн	High Level Input Current	$V_{CC} = 5.5V V_{IH} = 2.7V$			-1-1	20	μΑ
l <sub>I</sub> L	Low Level Input Current	$V_{CC} = 5.5 V V_{IL} =$	= 0.4V			-0.2	m/
IO	Output Drive Current	V <sub>CC</sub> = 5.5V	54/74ALS V <sub>O</sub> = 2.25V	-30		-110	m/
lozh	Off-State Output Current, High Level Voltage Applied	$V_{CC} = 5.5V V_{IH}$ $V_{O} = 2.7V$	= 2V			20	μА
lozL	Off-State Output Current, Low Level Voltage Applied	$V_{CC} = 5.5V V_{IH} = 0.4V$	$V_{CC} = 5.5V V_{IH} = 2V$ $V_{O} = 0.4V$			-20	μΑ
Icc	Supply Current	V <sub>CC</sub> = 5.5V	Outputs High		11	17	mA
		Outputs Open	Outputs Low		19	28	mA
			Outputs Disabled		20	31	mA

Parameter	From	То	Conditions	DM54ALS534			DM74ALS534			
				Min	Тур	Max	Min	Тур	Max	Unit
FMAX				30			35			MHz
TPLH	Clock	Any Q	$V_{CC}=4.5V$ to 5.5V $R_L=500~\Omega$ $C_L=50~pF$	4		15	4		12	ns
T <sub>PHL</sub>				4		15	4		12	ns
T <sub>PZH</sub>	Output Control	Any Q		3		18	4		15	ns
TPZL				4		21	5		18	ns
T <sub>PHZ</sub>				2		12	2		10	ns
TPLZ				3		15	3	152 28	13	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-5.

#### **Logic Diagram**



#### **Function Table**

Output Control	Clock	D	Output Q
L	1	Н	L
L	1	L	Н
L	L	X	Q <sub>0</sub>
Н	X	X	Z

L = Low State, H = High State, X = Don't Care

† = Positive Edge Transition

Z = High Impedance State

\$\tilde{Q}\_0\$ = Previous Condition of \$\tilde{Q}\$

## DM54ALS/DM74ALS563,564 TRI-STATE® Inverting Octal D-Type Latches and Edge-Triggered Flip-Flops

#### **Features**

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- 3-State Buffer-Type Outputs Drive Bus Lines Directly.

The ALS563 is identical to the ALS580. For detailed specification, refer to ALS580 data sheet. The ALS564 is identical to the ALS576. For detailed specification, refer to ALS576 data sheet.



Preliminary

### DM54ALS573/DM74ALS573 Octal D-Type Transparent Latches

#### **General Description**

These 8-bit registers feature totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the ALS573 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was set up.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches. That is, the old data can be retained or new data can be entered even while the outputs are off.

#### **Features**

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally Equivalent with LS373.
- Improved AC Performance Over LS373 at Approximately Half the Power.
- 3-State Buffer-Type Outputs Drive Bus Lines Directly.

#### **Absolute Maximum Ratings**

 Supply Voltage
 7V

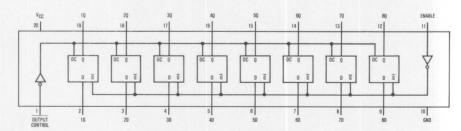
 Input Voltage
 7V

 Operating Free Air Temperature Range
 —55°C to 125°C

 DM54ALS573
 —55°C to 70°C

 DM74ALS573
 0°C to 70°C

 Storage Temperature Range
 —65°C to 150°C



54ALS573 (J) 74ALS573 (J,N)

	D	M54ALS5	73	D	M74ALS5	73	
Parameter	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, VCC	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, VIH	2	William.		2			V
Low Level Input Voltage, VIL		Files you	0.8	E FILE		0.8	V
High Level Output Voltage, VOH			5.5			5.5	V
High Level Output Current, IOH			-1.0			-2.6	mA
Low Level Output Current, IOL			12			24	mA
Width of Enable Pulse, High or Low	10			10	mby the		ns
Data Setup Time, T <sub>SU</sub>	10↓			10↓		don	ns
Data Hold Time, T <sub>H</sub>	7↓			7↓			ns

The (1) arrow indicates the negative edge of the enable is used for reference.

#### Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Тур	Max	Uni
VIK	Input Clamp Voltage	V <sub>CC</sub> = 4.5V I <sub>I</sub> =	-18mA		P PN AND	-1.5	V
Vон	High Level Output Voltage	$V_{CC} = 4.5V$ $V_{IL} = V_{IL} MAX$	54/74ALS I <sub>OH</sub> = -1mA	2.4	3.2		V
			$74ALS$ $I_{OH} = -2.6mA$	2.4	3.3		V
		$I_{OH} = -400\mu A$	54/74ALS	V <sub>CC</sub> -2			V
VOL	Low Level Output Voltage	V <sub>CC</sub> = 4.5V V <sub>IH</sub> = 2V	54/74ALS I <sub>OL</sub> = 12mA		0.25	0.4	٧
		74ALS I <sub>OL</sub> = 24mA		0.35	0.5	V	
lį	Max High Input Current	$V_{CC} = 5.5V V_{IH}$			0.1	mA	
IIH	High Level Input Current	$V_{CC} = 5.5V V_{IH}$			20	μΑ	
IIL	Low Level Input Current	$V_{CC} = 5.5V V_{IL} = 0.4V$				-0.2	mA
10	Output Drive Current	V <sub>CC</sub> = 5.5V	54/74ALS V <sub>O</sub> = 2.25V	-30		-110	mA
lozh	Off-State Output Current, High Level Voltage Applied	$V_{CC} = 5.5V V_{IH} = V_{O} = 2.7V$	= 2V			20	μΑ
lozL	Off-State Output Current, Low Level Voltage Applied	$V_{CC} = 5.5V V_{IH} = 0.4V$	$V_{CC} = 5.5V V_{IH} = 2V$ $V_{O} = 0.4V$			-20	μΑ
lcc	Supply Current	V <sub>CC</sub> = 5.5V	Outputs High		10	14	mA
		Outputs Open Outputs Low			15	22	mA
			Outputs Disabled		15.5	24	mA

#### Switching Characteristics over recommended operating free air temperature range (Note 1)

				DM54ALS573			Di			
Parameter	Parameter From To Conditions	Conditions	Min	Тур	Max	Min	Тур	Max	Unit	
TPLH	Data	Any Q		2		15	2		12	ns
TPHL	Dutu	/ my Q	$V_{CC} = 4.5V \text{ to } 5.5V$ $R_{L} = 500 \Omega$	2		15	2		12	ns
TPLH	Enable	Any Q		8		27	8		20	ns
TPHL		, ~		8		20	8		19	ns
TPZH			$C_L = 50 \text{ pF}$	4		21	4		18	ns
TPZL	Output	Any Q		4		21	5		18	ns
TPHZ	Control	Ally Q		2		10	2		8	ns
TPLZ				3		15	3		13	ns

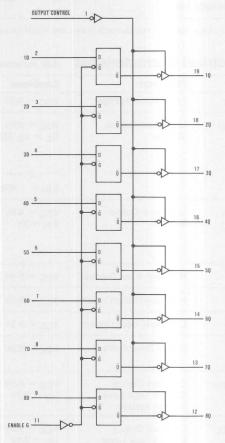
NOTE 1: See notes pg. 1-iii, figures pg. 3-5.

#### **Function Table**

Output Control	Enable G	D	Output Q
L	Н	Н	Н
L	Н	L	L
L	L	X	Q <sub>0</sub>
Н	X	X	Z

L = Low State, H = High State, X = Don't Care Z = High Impedance State  $Q_0 = Previous Condition of Q$ 

#### **Logic Diagram**





### DM54ALS574/DM74ALS574 Octal D-Type Edge-Triggered Flip-Flops

#### **General Description**

These 8-bit registers feature totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the ALS574 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

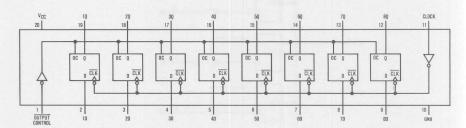
#### **Features**

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally Equivalent with LS374.
- Improved AC Performance Over LS374 at Approximately Half the Power.
- 3-State Buffer-Type Outputs Drive Bus Lines Directly.

#### **Absolute Maximum Ratings**

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS574	-55°C to 125°C
DM74ALS574	0°C to 70°C
Storage Temperature Range	-65°C to 150°C

#### **Connection Diagram**



54ALS574 (J)

74ALS574 (J,N)

#### **Function Table**

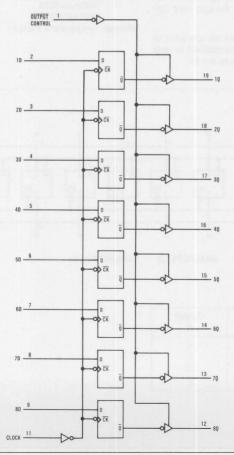
Output Control	Clock	D	Output
L	1	Н	Н
L	1	L	L
L	L	X	Q <sub>0</sub>
Н	X	X	Z

- L = Low State, H = High State, X = Don't Care
- $\uparrow = \text{Positive Edge Transition}$
- Z = High Impedance State

		D	M54ALS5	74	D	M74ALS57	74	
Parameter		Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, V <sub>CC</sub>		4.5	5	5 5.5	4.5	5	5.5	V
High Level Input Voltage, VIH		2	ME BE		2	(2001)		٧
Low Level Input Voltage, VIL				0.8	ranife.		0.8	٧
High Level Output Voltage, VOH				5.5			5.5	٧
High Level Output Current, IOH			lanu Segu	-1.0	gelille Had Lab		-2.6	mA
Low Level Output Current, IOL				12			24	m.A
Clock frequency, fCLOCK	umipa yawatan	0		30	0		35	МН
Width of Clock Pulse, Tw	High	10			10	Tales A.		ns
Albandan San Basan Albandan Basan	Low	17			15	di per	1234	ns
Data Setup Time, T <sub>SU</sub>		10↑			10↑		33	ns
Data Hold Time, TH		4↑	Reals - 12	au at re	01			ns

The (†) arrow indicates the positive edge of the Clock is used for reference.

#### **Logic Diagram**



15.5

27

mA

	Parameter	Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Voltage	V <sub>CC</sub> = 4.5V I <sub>I</sub> =	-18mA			-1.5	V
Vон	High Level Output Voltage	$V_{CC} = 4.5V$ $V_{IL} = V_{IL} MAX$	54/74ALS I <sub>OH</sub> = -1mA	2.4	3.2	68.14	٧
	strate		$74ALS$ $I_{OH} = -2.6mA$	2.4	3.3	POIN E	V
		$I_{OH} = -400\mu A$	54/74ALS	V <sub>CC</sub> -2		raneG	V
VOL	Low Level Output Voltage	$V_{CC} = 4.5V$ $V_{IH} = 2V$	54/74ALS I <sub>OL</sub> = 12mA		0.25	0.4	V
tgrafil July vertical balestonic pa		74ALS I <sub>OL</sub> = 24mA		0.35	0.5	V	
lį	Max High Input Current	$V_{CC} = 5.5V V_{IH} = 7V$				0.1	mA
lін	High Level Input Current	$V_{CC} = 5.5 V V_{IH}$	= 2.7V			20	μΑ
IIL	Low Level Input Current	V <sub>CC</sub> = 5.5V V <sub>IL</sub> =	= 0.4V			-0.2	mA
10	Output Drive Current	$V_{CC} = 5.5V$	54/74ALS V <sub>O</sub> = 2.25V	-30		-110	mA
lozh	Off-State Output Current, High Level Voltage Applied	$V_{CC} = 5.5V V_{IH} = V_{O} = 2.7V$	= 2V			20	μΑ
lozL	Off-State Output Current, Low Level Voltage Applied	$V_{CC} = 5.5V V_{IH} = 0.4V$	$V_{CC} = 5.5V V_{IH} = 2V$ $V_{O} = 0.4V$			-20	μΑ
Icc	Supply Current	V <sub>CC</sub> = 5.5V	Outputs High		10.5	17	mA
		Outputs Open	Outputs Low		14.5	23	mA

#### Switching Characteristics over recommended operating free air temperature range (Note 1)

				DM54ALS574			DM74ALS574			
Parameter	From	То	Conditions	Min	Тур	Max	Min	Тур	Max	Unit
FMAX				30			35			MHz
TPLH	Clock	Any Q	$V_{CC} = 4.5V \text{ to } 5.5V$ $R_L = 500 \Omega$	4		15	4		12	ns
T <sub>PHL</sub>		,		4		15	4		12	ns
TPZH	Output	Any Q		4		21	5		18	ns
TPZL	Control	, -	$C_L = 50 \text{ pF}$	4		21	5		18	ns
T <sub>PHZ</sub>	Output	Any Q	(KIN MISCANI)	2	THE THE	10	2		8	ns
TPLZ	Control	, ~		3		15	3		13	ns

Outputs Disabled

NOTE 1: See notes pg. 1-iii, figures pg. 3-5.

Preliminary

#### DM54ALS576/DM74ALS576 Octal D-Type Edge-Triggered Flip-Flops With Inverted Outputs

#### **General Description**

These 8-bit registers feature totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the ALS576 are edge-triggered inverting D-type flip-flops. On the positive transition of the clock, the  $\overline{\mathbb{Q}}$  outputs will be set to the complement of the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

#### **Features**

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- 3-State Buffer-Type Outputs Drive Bus Lines Directly.

#### **Absolute Maximum Ratings**

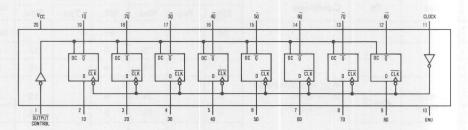
 Supply Voltage
 7V

 Input Voltage
 7V

 Operating Free Air Temperature Range
 —55°C to 125°C

 DM54ALS576
 —0°C to 70°C

 Storage Temperature Range
 —65°C to 150°C



54ALS576 (J) 74ALS576 (J,N)

		D	M54ALS5	76	D			
Parameter		Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, V <sub>CC</sub>		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, VIH		2	To the last	0 - 5 1 <u>1</u> <u>1</u> <u>1</u> <u>1</u> <u>1</u> <u>1</u> <u>1</u> <u>1</u> <u>1</u> <u></u>	2		and the	V
Low Level Input Voltage, VIL	to to			0.8			0.8	V
High Level Output Voltage, VOH	oaW L	e male in	Augito i	5.5			5.5	V
High Level Output Current, IOH				-1.0		iele Ques	-2.6	mA
Low Level Output Current, IOL				12			24	mA
Clock frequency, fCLOCK		0		30	0		35	МН
Width of Clock Pulse, Tw	High	10		100	10			ns
	Low	17			15		J. right	ns
Data Setup Time, T <sub>SU</sub>		10↑			10↑		I WOL	ns
Data Hold Time, T <sub>H</sub>		4↑	1 1994		01	per per li	mino /	ns

The (†) arrow indicates the positive edge of the Clock is used for reference.

	Parameter	Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Voltage	V <sub>CC</sub> = 4.5V I <sub>I</sub> =	-18mA			-1.5	V
Vон	High Level Output Voltage	V <sub>CC</sub> = 4.5V V <sub>IL</sub> = V <sub>IL</sub> MAX	54/74ALS I <sub>OH</sub> = -1mA	2.4	3.2	,	V
	80		74ALS I <sub>OH</sub> = -2.6mA	2.4	3.3		٧
	48	$I_{OH} = -400\mu A$	54/74ALS	V <sub>CC</sub> -2		a ist fin	V
VOL	Low Level Output Voltage	V <sub>CC</sub> = 4.5V V <sub>IH</sub> = 2V	54/74ALS I <sub>OL</sub> = 12mA	140	0.25	0.4	٧
	May High Input Current Voc - 5 5V VV		74ALS I <sub>OL</sub> = 24mA		0.35	0.5	V
lį	Max High Input Current	$V_{CC} = 5.5V V_{IH}$			0.1	mA	
ΊΗ	High Level Input Current	$V_{CC} = 5.5V V_{IH}$			20	μΑ	
IIL	Low Level Input Current	$V_{CC} = 5.5 V V_{IL}$	= 0.4V			-0.2	mA
IO	Output Drive Current	$V_{CC} = 5.5V$	54/74ALS V <sub>O</sub> = 2.25V	-30		-110	mA
lozh	Off-State Output Current, High Level Voltage Applied	$V_{CC} = 5.5V V_{IH}$ $V_{O} = 2.7V$	= 2V			20	μΑ
IOZL	Off-State Output Current, Low Level Voltage Applied	$V_{CC} = 5.5V V_{IH}$ $V_{O} = 0.4V$	= 2V			-20	μΑ
Icc	Supply Current	V <sub>CC</sub> = 5.5V	Outputs High		10.5	17	mA
		Outputs Open	Outputs Low		14.5	23	mA
			Outputs Disabled		15.5	27	mA

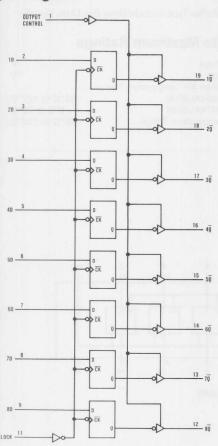
Switching (	haract	teristics
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over recommended operating free air temperature range (Note 1)

			One dialone	DI	M54ALS	576	DI	DM74ALS576		
Parameter From 1	То	Conditions	Min	Тур	Max	Min	Тур	Max	Unit	
FMAX				30			35			MHz
TPLH	Clock	Any Q		4		15	4		12	ns
T <sub>PHL</sub>	0.001	7.1.1, 0		4		15	4		12	ns
T <sub>PZH</sub>	Output	Any Q	$V_{CC} = 4.5 \text{V to } 5.5 \text{V}$ $R_L = 500 \Omega$	4		21	4	Malle	18	ns
TPZL	Control	7, 4	$C_L = 50 \text{ pF}$	4		21	4		18	ns
T <sub>PHZ</sub>			Pentures	2	ne sessi banker	10	2		8	ns
TPLZ				3		15	3		13	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-5.

#### **Logic Diagram**



#### **Function Table**

Output Control	Clock	D	Output Q
L	1	Н	L
L	1	L	Н
L	L L	X	Q <sub>0</sub>
Н	X	X	Z

L = Low State, H = High State, X = Don't Care

↑ = Positive Edge Transition

z = High Impedance State $\bar{Q}_0 = \text{Previous Condition of } \bar{Q}$ 

National Semiconductor

Preliminary

## DM54ALS580/DM74ALS580 Octal D-Type Transparent Latches With Inverted Outputs

#### **General Description**

These 8-bit registers feature totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight inverting latches of the ALS580 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the complement of the data (D) inputs. When the enable is taken low the output will be latched at the complement of the level of the data that was set up.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches. That is, the old data can be retained or new data can be entered even while the outputs are off.

#### **Features**

- Switching Specifications at 50pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced, Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- 3-State Buffer-Type Outputs Drive Bus Lines Directly.

#### **Absolute Maximum Ratings**

 Supply Voltage
 7V

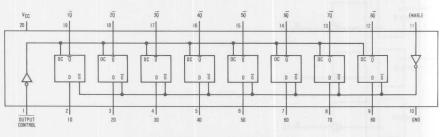
 Input Voltage
 7V

 Operating Free Air Temperature Range
 —55°C to 125°C

 DM54ALS580
 —55°C to 70°C

 DM74ALS580
 0°C to 70°C

 Storage Temperature Range
 —65°C to 150°C



54ALS580 (J) 74ALS580 (J,N)

	D	M54ALS5	80	D	30		
Parameter	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, V <sub>CC</sub>	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, VIH	2			2			V
Low Level Input Voltage, VIL			0.8			0.8	V
High Level Output Voltage, VOH			5.5			5.5	V
High Level Output Current, IOH			-1.0	Ours		-2.6	mA
Low Level Output Current, IOL			12			24	mA
Width of Enable Pulse, High or Low	15			15			ns
Data Setup Time, T <sub>SU</sub>	101			10↓			ns
Data Hold Time, T <sub>H</sub>	01			01			ns

The (1) arrow indicates the negative edge of the enable is used for reference.

#### Electrical Characteristics over recommended operating free air temperature range (Note 1)

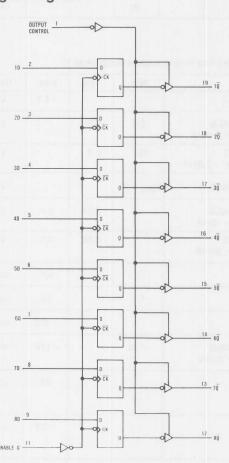
	Parameter	Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Voltage	V <sub>CC</sub> = 4.5V I <sub>I</sub> =	-18mA			-1.5	V
VOH	High Level Output Voltage			2.4	3.2		V
			$74ALS$ $I_{OH} = -2.6mA$	2.4	3.3		V
		$I_{OH} = -400\mu A$	54/74ALS	V <sub>CC</sub> -2			٧
VOL	Low Level Output Voltage	$V_{CC} = 4.5V$ $V_{IH} = 2V$	54/74ALS I <sub>OL</sub> = 12mA		0.25	0.4	٧
			74ALS I <sub>OL</sub> = 24mA		0.35	0.5	V
l <sub>l</sub>	Max High Input Current	V <sub>CC</sub> = 5.5V V <sub>IH</sub>			0.1	mA	
ΊΗ	High Level Input Current	$V_{CC} = 5.5 V V_{IH} = 2.7 V$				20	μΑ
IIL	Low Level Input Current	$V_{CC} = 5.5V V_{IL} =$	= 0.4V			-0.2	mA
10	Output Drive Current	V <sub>CC</sub> = 5.5V	54/74ALS V <sub>O</sub> = 2.25V	-30		-110	mA
lozh	Off-State Output Current, High Level Voltage Applied	$V_{CC} = 5.5V V_{IH} = 0.000$ $V_{O} = 2.7V$	= 2V			20	μΑ
lozL	Off-State Output Current, Low Level Voltage Applied	$V_{CC} = 5.5V V_{IH} = 0.4V$	= 2V			-20	μΑ
Icc	Supply Current	V <sub>CC</sub> = 5.5V	Outputs High		10	16	mA
		Outputs Open	Outputs Low		15	24	mA
			Outputs Disabled		15.5	26	mA

#### Switching Characteristics over recommended operating free air temperature range (Note 1)

				DM54ALS580			DI	7		
Parameter	From	То	Conditions	Min	Тур	Max	Min	Тур	Max	Unit
TPLH	Data	Any Q		3		21	3		18	ns
TPHL			V <sub>CC</sub> = 4.5V to 5.5V R <sub>L</sub> = 500 Ω	3		15	3		12	ns
TPLH	Enable	Any Q		8		27	8		22	ns
TPHL		Enable Any Q		8		22	8		21	ns
TPZH			$C_L = 50 \text{ pF}$	4		21	4		18	ns
TPZL	Output	Any Q		4		21	4		18	ns
TPHZ	Control	7, ~		2		10	2		8	ns
TPLZ				3		15	3		13	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-5.

#### **Logic Diagram**



#### **Function Table**

Output Control	Enable G	D	Output Q
L	Н	Н	L
L	Н	L	Н
L	L	X	Q <sub>0</sub>
Н	X	X	Z

 $L = Low State, H = High State, X = Don't Care Z = High Impedance State <math>\bar{Q}_0 = Previous Condition of \bar{Q}$ 

#### DM54ALS/DM74ALS689 8-Bit Comparator

#### **General Description**

This comparator performs an ''equal to'' comparison of two eight-bit words with provision for expansion or external enabling. The matching of the two 8-bit input plus a logic LOW on the  $\overline{\text{EN}}$  input produces the output  $\overline{\text{A}}=\overline{\text{B}}$ . The ALS 689 has an open collector output for wire AND cascading.

#### **Features**

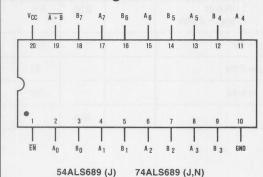
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.

- Functionally and Pin for Pin Compatible with LS Family TTL Counterpart.
- Improved Output Transient Handling Capability.

#### **Absolute Maximum Ratings**

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54ALS689	-55°C to 125°C
DM74ALS689	0°C to 70°C
Storage Temperature Range	-65°C to 150°C

#### **Connection Diagram**



#### **Function Table**

In	outs	Output
EN	Data	A=B
L	A=B	L
L	A≠B	Н
Н	X	Н

H = High Level, L = Low Level, X = Don't Care

	DM54ALS689				DM74ALS689			
Parameter	Min	Nom	Max	Min	Nom	Max	Unit	
Supply Voltage, V <sub>CC</sub>	4.5	5	5.5	4.5	5	5.5	V	
High Level Input Voltage, VIH	2			2			V	
Low Level Input Voltage, VIL			0.8			0.8	V	
High Level Output Voltage, VOH		tato we 19	5.5			5.5	V	
Low Level Output Current, IOL	Jointon and		12			24	mA	

#### Electrical Characteristics over recommended operating free air temperature range (Note 1)

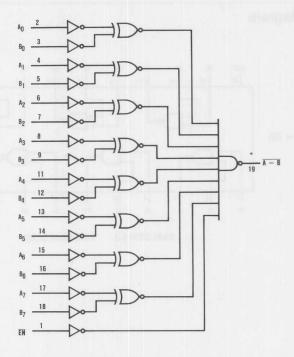
	Parameter	Conditions	Min	Тур	Max	Unit	
VIK	Input Clamp Voltage	V <sub>CC</sub> = 4.5V, I <sub>I</sub> =	-18mA	incom a		-1.5	V
ЮН	High Level Output Current	$V_{CC} = 4.5V, V_{OH}$	H = 5.5V			100	μΑ
VOL Low Level Output Voltage	$V_{CC} = 4.5V$	54/74ALS I <sub>OL</sub> = 12mA	nante	0.25	0.4	V	
		74ALS I <sub>OL</sub> = 24mA	4 14	0.35	0.5	V	
l <sub>l</sub>	Max High Input Current	$V_{CC} = 5.5V, V_{IH}$	= 7V			100	μΑ
ΙΗ	High Level Input Current	$V_{CC} = 5.5V, V_{IH}$	= 2.7V			20	μΑ
IIL	Low Level Input Current	$V_{CC} = 5.5V, V_{IL} = 0.4V$				-200	μΑ
Icc	Supply Current	$V_{CC} = 5.5V$			10.5		mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

	From	To Output	Conditions	DM54ALS689			DM74ALS689				
Parameter	Input			Min	Тур	Max	Min	Тур	Max	Unit	
TPLH, Propagation Delay Time, Low to high Level Output	A or B		V <sub>CC</sub> : 4.5V to 5.5V C <sub>L</sub> = 50pF R <sub>L</sub> = 667Ω	Maid 24	3	13	31	3	13	23	
T <sub>PHL</sub> , Propagation Delay Time, High to low Level Output	Data			4	12	30	4	12	24		
TPLH, Propagation Delay Time, Low to high Level Output	ĒN	A=B		3	12	29	3	12	21	ns	
TPHL, Propagation Delay Time, High to low Level Output		76 185		3	10	24	3	10	20		

NOTE 1: See notes pg. 1-iii, figures pg 3-4.

#### **Logic Diagram**



\* Output is open collector

**Preliminary** 

7V

7V

#### DM54ALS804/DM74ALS804 Hex 2-Input NAND Drivers

#### **Features**

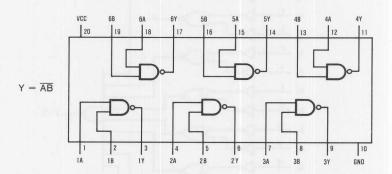
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin for Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

#### **Absolute Maximum Ratings**

Supply Voltage
Input Voltage

Operating Free Air Temperature Range
DM54ALS -55°C to 125°C

DM74ALS 0°C to 70°C Storage Temperature Range -65°C to 150°C



54ALS804 (J) 74ALS804 (J,N)

	D	M54ALS8	04	D	04	111-14	
Parameter	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, VCC	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, VIH	2			2			V
Low Level Input Voltage, VIL			0.8			0.8	V
High Level Output Current, IOH	and toy light		-1.0		un men	-2.6	mA
Low Level Output Current, IOL	nhet/	JET	12	enselomi e		24	mA

#### Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Тур	Max	Uni
VIK	Input Clamp Voltage	$V_{CC} = 4.5V$ , $I_I = -18$ mA				-1.5	V
VOH	High Level Output	$I_{OH} = -0.4$ mA		V <sub>CC</sub> -2	neren	i goi:	V
	Voltage	I <sub>OH</sub> = MAX		2.4			V
VOL	Low Level Output Voltage	$V_{CC} = 4.5V$	54/74ALS I <sub>OL</sub> = 12mA		0.25	0.4	V
			74 ALS IOL = 24mA		0.35	0.5	V
l <sub>I</sub>	Max High Input Current	$V_{CC} = 5.5V, V_{IH}$	= 7V			0.1	mA
lін	High Level Input Current	$V_{CC} = 5.5V, V_{IH}$	= 2.7V			20	μΑ
կլ	Low Level Input Current	$V_{CC} = 5.5V, V_{IL}$	= 0.4V			-0.2	mA
10	Output Drive Current	$V_{CC} = 5.5V$	V <sub>O</sub> = 2.25V	-30		-110	mA
lcc	Supply Current	$V_{CC} = 5.5V$	Outputs High		0.14		mA
		(M.Y.) HORSTINAL	Outputs Low		1.2		mA

#### Switching Characteristics over recommended operating free air temperature range (Note 1)

		DM54ALS804			D			
Parameter	Conditions	Min	Тур	Max	Min	Тур	Max	Unit
TPLH, Propagation delay time. Low to high level output	$V_{CC} = 4.5 \text{ to } 5.5V$ $R_L = 500 \Omega,$ $C_L = 50 \text{pF}.$	1.4	2.9	7.0	1.4	2.9	6.0	ns
TPHL, Propagation delay time. High to low level output		1.2	2.5	6.0	1.2	2.5	5.0	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-1.

#### **Features**

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin for Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

#### **Absolute Maximum Ratings**

Supply Voltage

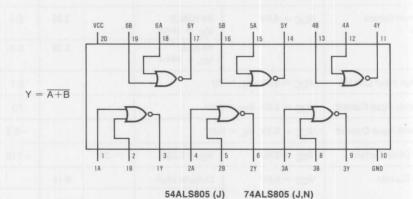
Input Voltage
Operating Free Air Temperature Range

DM54ALS DM74ALS

Storage Temperature Range

7V 7V

-55°C to 125°C 0°C to 70°C -65°C to 150°C



	D	M54ALS8	05	D	M74ALS8	05	
Parameter	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, VCC	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, VIH	2			2			V
Low Level Input Voltage, VIL			0.8			0.8	V
High Level Output Current, IOH			-1.0			-2.6	mA
Low Level Output Current, IOL	Catalan	Jan-	12	binutiers.		24	mA

#### Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Voltage	$V_{CC} = 4.5V, I_{I} = -18mA$				-1.5	V
VOH	High Level Output	$I_{OH} = -0.4$ mA		V <sub>CC</sub> -2		I non:	V
	Voltage	I <sub>OH</sub> = MAX		2.4			V
VOL	Low Level Output Voltage	V <sub>CC</sub> = 4.5V	54/74ALS I <sub>OL</sub> = 12mA	in the	0.25	0.4	V
			74 ALS I <sub>OL</sub> = 24mA		0.35	0.5	V
l <sub>l</sub>	Max High Input Current	$V_{CC} = 5.5V, V_{IH}$	= 7V			0.1	mA
ΊΗ	High Level Input Current	$V_{CC} = 5.5V, V_{IH}$	= 2.7V			20	μΑ
IIL	Low Level Input Current	$V_{CC} = 5.5V, V_{IL}$	= 0.4V			-0.2	mA
IO	Output Drive Current	V <sub>CC</sub> = 5.5V	V <sub>O</sub> = 2.25V	-30		-110	mA
ICC	Supply Current	$V_{CC} = 5.5V$	Outputs High		0.28		mA
		Holling Charles	Outputs Low		1.4		m/

#### Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter		DM54ALS805			D			
	Conditions	Min	Тур	Max	Min	Тур	Max	Unit
TPLH, Propagation delay time. Low to high Level Output	$V_{CC} = 4.5 \text{ to } 5.5V$ $R_L = 500 \Omega$ , $C_L = 50 \text{ pF}$ .	1.7	3.4	8.5	1.7	3.4	7.0	ns
TPHL, Propagation delay time. High to low Level Output		1.2	2.5	6.5	1.2	2.5	5.0	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-1.

#### DM54ALS808/DM74ALS808 Hex 2-Input AND Drivers

#### **Features**

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin for Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

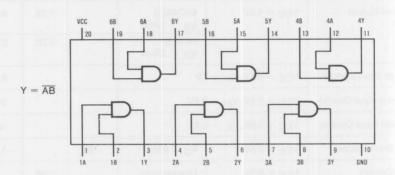
#### **Absolute Maximum Ratings**

Supply Voltage 7V
Input Voltage 7V
Operating Free Air Temperature Range

 DM54ALS
 -55°C to 125°C

 DM74ALS
 0°C to 70°C

 Storage Temperature Range
 -65°C to 150°C



54ALS808 (J) 74ALS808 (J,N)

	D	M54ALS8	08	D	08		
Parameter	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, VCC	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, VIH	2	45 - F.F		2			٧
Low Level Input Voltage, V <sub>IL</sub>			0.8			0.8	٧
High Level Output Current, IOH			-1.0		ends o marin	-2.6	mA
Low Level Output Current, IOL	C Leading Co.		12		pi menin	24	mA

#### Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Тур	Max	Uni
VIK	Input Clamp Voltage	$V_{CC} = 4.5V$ , $I_{I} = -18mA$				-1.5	٧
VOH	High Level Output	$I_{OH} =4mA$		V <sub>CC</sub> -2		I main	V
	Voltage	I <sub>OH</sub> = MAX		2.4			V
VOL	Low Level Output Voltage	V <sub>CC</sub> = 4.5V	54/74ALS I <sub>OL</sub> = 12mA		0.25	0.4	٧
			74 ALS I <sub>OL</sub> = 24mA		0.35	0.5	V
Ц	Max High Input Current	$V_{CC} = 5.5V, V_{IH}$	= 7V			0.1	mA
ΙΗ	High Level Input Current	$V_{CC} = 5.5V, V_{IH}$	= 2.7V			20	μΑ
IIL	Low Level Input Current	$V_{CC} = 5.5V, V_{IL}$	= 0.4V			-0.2	mA
10	Output Drive Current	$V_{CC} = 5.5V$	V <sub>O</sub> = 2.25V	-30		-110	mA
ICC	Supply Current	$V_{CC} = 5.5V$	Outputs High	10 100	0.53		mA
	A STATE OF THE STA	nito-ciul	Outputs Low		1.3		mA

#### Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter		DM54ALS808			D			
	Conditions	Min	Тур	Max	Min	Тур	Max	Unit
TPLH, Propagation delay time. Low to high Level Output	$V_{CC} = 4.5 \text{ to } 5.5V$ $R_L = 500 \Omega$ , $C_L = 50 \text{ pF}$ .	2.0	3.9	10.0	2.0	3.9	8.0	ns
TPHL, Propagation delay time. High to low Level Output		2.3	4.6	11.5	2.3	4.6	9.5	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-1.

National Semiconductor

Preliminary

#### DM54ALS832/DM74ALS832 Hex 2-Input OR Drivers

#### **Features**

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin for Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

#### **Absolute Maximum Ratings**

Supply Voltage Input Voltage

Operating Free Air Temperature Range

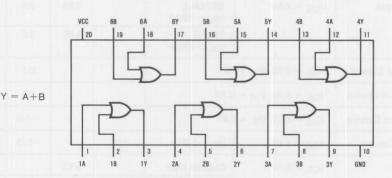
DM54ALS DM74ALS -55°C to 125°C 0°C to 70°C

7V

7V

Storage Temperature Range -65°C to 150°C

#### **Connection Diagram**



54ALS832 (J)

74ALS832 (J,N)

	D	M54ALS8	32	D			
Parameter	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, VCC	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, VIH	2	1000	BOREAU	2	WE		٧
Low Level Input Voltage, VIL			0.8			0.8	V
High Level Output Current, IOH			-1.0	-chalet in		-2.6	mA
Low Level Output Current, IOL		1 2 2 3 3 3	12			24	mA

#### Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Voltage	$V_{CC} = 4.5V, I_{I} = -18mA$				-1.5	V
Vон	High Level Output	$I_{OH} =4mA$	and the second	V <sub>CC</sub> -2		elsel repe	V
	Voltage	I <sub>OH</sub> = MAX		2.4		of human	V
VOL	Low Level Output Voltage	V <sub>CC</sub> = 4.5V	54/74ALS I <sub>OL</sub> = 12mA		0.25	0.4	٧
	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1		74 ALS IOL = 24mA		0.35	0.5	V
lį	Max High Input Current	V <sub>CC</sub> = 5.5V, V <sub>IH</sub>	= 7V	tir ablem	are nata	0.1	mA
lін	High Level Input Current	V <sub>CC</sub> = 5.5V, V <sub>IH</sub>	= 2.7V			20	μΑ
IIL	Low Level Input Current	$V_{CC} = 5.5V, V_{IL}$	= 0.4V			-0.2	mA
10	Output Drive Current	V <sub>CC</sub> = 5.5V	V <sub>O</sub> = 2.25V	-30		-110	mA
Icc	Supply Current	V <sub>CC</sub> = 5.5V	Outputs High		0.7		mA
			Outputs Low		1.4	uliui I	mA

### Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter		DM54ALS832			D			
	Conditions	Min	Тур	Max	Min	Тур	Max	Unit
TPLH, Propagation delay time. Low to high Level Output	$V_{CC} = 4.5 \text{ to } 5.5V$ $R_L = 500 \Omega,$ $C_L = 50 \text{pF}.$	2.0	3.9	10.0	2.0	3.9	8.0	ns
TPHL, Propagation delay time. High to low Level Output		2.5	5.1	9.0	2.5	5.1	10.5	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-1.



### DM54ALS873/DM74ALS873 Dual 4-Bit D-Type Transparent Latches

#### **General Description**

These Dual 4-Bit registers feature totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the ALS873 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was set up.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output conrol does not affect the internal operation of the latches. That is, the old data can be retained or new data can be entered even while the outputs are off.

#### **Features**

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- 3-State Buffer-Type Outputs Drive Bus Lines Directly.
- Space Saving 300 Mil Wide Package.

#### **Absolute Maximum Ratings**

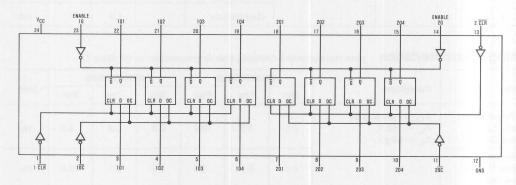
 Supply Voltage
 7V

 Input Voltage
 7V

 Operating Free Air Temperature Range
 —55°C to 125°C

 DM74ALS873
 —0°C to 70°C

 Storage Temperature Range
 —65°C to 150°C



54ALS873 (J) 74ALS873 (J,N)

	0	M54ALS8	73	D	M74ALS8	73	
Parameter	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, V <sub>CC</sub>	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, VIH	2			2			V
Low Level Input Voltage, VIL			0.8			0.8	V
High Level Output Voltage, VOH			5.5			5.5	V
High Level Output Current, IOH			-1.0			-2.6	mA
Low Level Output Current, IOL	Acadim in the second		12			24	mA
Pulse Width, T <sub>W</sub> Enable High Clear Low	10 15		E legy	10 15	raspi m	Hailey I	ns
Data Setup Time, T <sub>SU</sub>	101			10↓		I HER	ns
Data Hold Time, TH	7↓		101	7↓			ns

The (1) arrow indicates the negative edge of the enable is used for reference.

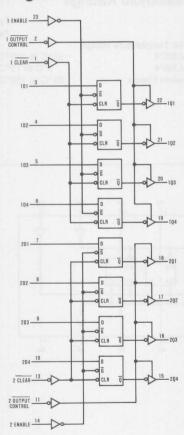
	Parameter	Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Voltage	V <sub>CC</sub> = 4.5V I <sub>I</sub> =	-18mA			-1.5	V
VOH High Level Output Voltage	V <sub>CC</sub> = 4.5V V <sub>IL</sub> = V <sub>IL</sub> MAX	54/74ALS IOH = -1mA	2.4	3.2	16115	V	
	3		74ALS I <sub>OH</sub> = -2.6mA	2.4	3.3		V
		$I_{OH} = -400\mu A$	54/74ALS	V <sub>CC</sub> -2			٧
VOL	Low Level Output Voltage	V <sub>CC</sub> = 4.5V V <sub>IH</sub> = 2V	54/74ALS I <sub>OL</sub> = 12mA		0.25	0.4	٧
			74ALS I <sub>OL</sub> = 24mA		0.35	0.5	V
lį	Max High Input Current	V <sub>CC</sub> = 5.5V V <sub>IH</sub> = 7V				0.1	mA
liн	High Level Input Current	V <sub>CC</sub> = 5.5V V <sub>IH</sub> = 2.7V				20	μΑ
IIL	Low Level Input Current	V <sub>CC</sub> = 5.5V V <sub>IL</sub>	= 0.4V			-0.2	mA
10	Output Drive Current	$V_{CC} = 5.5V$	54/74ALS V <sub>O</sub> = 2.25V	-30		-110	mA
lozh	Off-State Output Current, High Level Voltage Applied	$V_{CC} = 5.5V V_{IH}$ $V_{O} = 2.7V$	= 2V			20	μΑ
lozL	Off-State Output Current, Low Level Voltage Applied	$V_{CC} = 5.5V V_{IH} = 2V$ $V_{O} = 0.4V$				-20	μΑ
Icc	Supply Current	V <sub>CC</sub> = 5.5V	Outputs High		10	21	mA
		Outputs Open Outputs Low			15	29	mA
				15.5	31	mA	

Switching Characteristics over recommended operating free air temperature range (Note 1)

				Di	M54ALS8	373	DM74ALS873			
Parameter From To	Conditions	Min	Тур	Max	Min	Тур	Max	Unit		
TPLH	Data	Any Q		2		15	2	ATE	12	ns
TPHL	Dutu	7 my G	and all the	2		15	2		12	ns
TPLH	Enable	Any O	Any Q $V_{CC} = 4.5V \text{ to } 5.5V$ $R_L = 500 \Omega$ 8	8		29	8		21	ns
TPHL	Lilabio	Ally Q		22	8		21	ns		
TPZH	Mr. O.C.			4		21	4	HAIR	18	ns
TPZL	Output	Any Q	Elitaring Saleravian	4	V ISSUE	21	4	rejou	18	ns
TPHZ	Control	7, 0	to say the market property of the	2	mad Sa	10	2		8	ns
TPLZ	noted some	ami-noi pi	A HORSE DAY OF THE PROPERTY OF	2	Ditt- like	15	2	terran	13	ns
TPHL	Clear	Any Q		6		24	6		24	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-5.

#### **Logic Diagram**



#### **Function Table**

CLR	D	EN	OC	G
X	X	X	Н	Z
L	X	X	L	L
Н	Н	Н	L	Н
Н	L	Н	L	L
H	X	L	L	Q <sub>0</sub>

L= Low State, H= High State, X= Don't Care Z= High Impedance State  $Q_0=$  Previous Condition of Q



### DM54ALS874/DM74ALS874 Dual 4-Bit D-Type Edge-Triggered Flip-Flops

#### **General Description**

These Dual 4-Bit registers feature totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the ALS874 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

#### **Features**

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- 3-State Buffer-Type Outputs Drive Bus Lines Directly.
- Space Saving 300 Mil Wide Package.

#### **Absolute Maximum Ratings**

 Supply Voltage
 7V

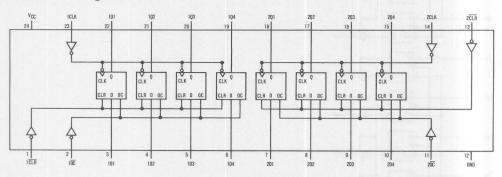
 Input Voltage
 7V

 Operating Free Air Temperature Range
 —55°C to 125°C

 DM54ALS874
 —55°C to 70°C

 DM74ALS874
 0°C to 70°C

 Storage Temperature Range
 —65°C to 150°C



54ALS874 (J) 74ALS874 (J,N)

		0	M54ALS8	74	D	M74ALS8	74	1
Parameter	Parameter		Nom	Max	Min	Nom	Max	Unit
Supply Voltage, V <sub>CC</sub>		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, VIH		2			2			V
Low Level Input Voltage, VIL	Mill			0.8			0.8	V
High Level Output Voltage, VOH				5.5			5.5	V
High Level Output Current, IOH				-1.0			-2.6	mA
Low Level Output Current, IOL				12			24	m.A
Clock frequency, fCLOCK		0		30	0		35	МН
Width of Clock Pulse, Tw	High	10			10			ns
	Low	17			15			ns
Width of Clear Pulse, T <sub>W</sub>		10			10			ns
Data Setup Time, T <sub>SU</sub>		10↑			10↑			ns
Data Hold Time, T <sub>H</sub>		41	in the	E ABY	01	Tassauro un	HE HO	ns

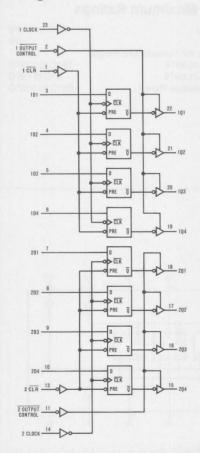
The (1) arrow indicates the positive edge of the Clock is used for reference.

	Parameter	Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Voltage	V <sub>CC</sub> = 4.5V I <sub>I</sub> =	-18mA			-1.5	٧
VOH High Level Output Voltage	$V_{CC} = 4.5V$ $V_{IL} = V_{IL} MAX$	54/74ALS I <sub>OH</sub> = -1mA	2.4	3.2		V	
			74ALS I <sub>OH</sub> = -2.6mA	2.4	3.3		V
		$I_{OH} = -400\mu A$	54/74ALS	V <sub>CC</sub> -2			٧
VOL	VOL Low Level Output Voltage	V <sub>CC</sub> = 4.5V V <sub>IH</sub> = 2V	54/74ALS I <sub>OL</sub> = 12mA		0.25	0.4	٧
Jan Hall		74ALS IOL = 24mA				0.5	٧
lį	Max High Input Current	V <sub>CC</sub> = 5.5V V <sub>IH</sub> = 7V				0.1	mA
ІІН	High Level Input Current	$V_{CC} = 5.5V V_{IH} = 2.7V$				20	μΑ
l <sub>IL</sub>	Low Level Input Current	V <sub>CC</sub> = 5.5V V <sub>IL</sub>	$V_{CC} = 5.5 V V_{IL} = 0.4 V$			-0.2	mA
10	Output Drive Current	V <sub>CC</sub> = 5.5V	54/74ALS V <sub>O</sub> = 2.25V	-30		-110	mA
lozh	Off-State Output Current, High Level Voltage Applied	$V_{CC} = 5.5V V_{IH}$ $V_{O} = 2.7V$	= 2V			20	μΑ
lozL	Off-State Output Current, Low Level Voltage Applied	$V_{CC} = 5.5V V_{IH} = 2V$ $V_{O} = 0.4V$				-20	μΑ
ICC	Supply Current	V <sub>CC</sub> = 5.5V Outputs Open	Outputs High		14	21	mA
		Outputs Open	Outputs Low		18	29	mA
			Outputs Disabled		20	31	mA

Parameter From To Conditi					DM54ALS874			DM74ALS874			
	Conditions	Min	Тур	Max	Min	Тур	Max	Unit			
FMAX				30	700		35		o in	MHz	
TPLH	Clock	Any Q		4		15	4		12	ns	
T <sub>PHL</sub>	0.001	7, C		4		15	4		12	ns	
T <sub>PZH</sub>	Output	Any Q	Any Q	$V_{CC} = 4.5V \text{ to } 5.5V$ $R_{L} = 500 \Omega$	4		21	4		18	ns
TPZL	Control			$C_L = 50 \text{ pF}$	4		21	4	Hali	18	ns
T <sub>PHZ</sub>		Name of		2		10	2		8	ns	
TPLZ	FILE SAME R	CONSTRUCTION IN		3	To the same	15	3	14 W W	13	ns	
TPHL	Clear	Any Q	nike interest to continue	6	1.100.25	22	6		19	ns	

NOTE 1: See notes pg. 1-iii, figures pg. 3-5.

#### **Logic Diagram**



#### **Function Table**

CLR	D	CLK	OC	Q
X	X	X	Н	Z
L	X	X	L	L
Н	Н	1	L	Н
Н	L	1 3 3 4 4	L	L
Н	X	L	L	Qo

L = Low State, H = High State, X = Don't Care

1 = Positive Edge Transition

2 = High Impedance State

Q<sub>0</sub> = Previous Condition of Q



# DM54ALS876/DM74ALS876 Dual 4-Bit D-Type Edge-Triggered Flip-Flops With Inverted Outputs

#### **General Description**

These inverting Dual 4-Bit registers feature totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the ALS876 are edge-triggered inverting D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the complement of the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

#### **Features**

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- 3-State Buffer-Type Outputs Drive Bus Lines Directly.
- Space Saving 300 Mil Wide Package.

#### **Absolute Maximum Ratings**

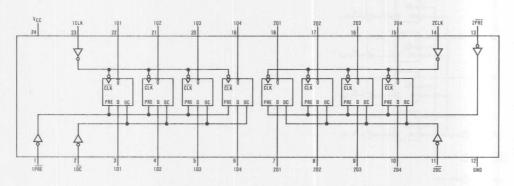
 Supply Voltage
 7V

 Input Voltage
 7V

 Operating Free Air Temperature Range
 —55°C to 125°C

 DM54ALS876
 —55°C to 70°C

 Storage Temperature Range
 —65°C to 150°C



54ALS876 (J) 74ALS876 (J,N)

Parameter		D	M54ALS8	76	D			
		Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, VCC		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, VIH		2	Talks 3		2		WHAK !	V
Low Level Input Voltage, VIL	3400			0.8			0.8	V
High Level Output Voltage, VOH		a Partial -	A.Jipa	5.5			5.5	V
High Level Output Current, IOH			The last	-1.0		Digno Chile	-2.6	mA
Low Level Output Current, IOL				12			24	mA
Clock frequency, fCLOCK		0		30	0		35	MHz
Width of Clock Pulse, Tw	High	10			10			ns
	Low	17			15			ns
Width of Preset Pulse, TW Low		10			10	d. sqrtt (hid		ns
Data Setup Time, T <sub>SU</sub>		10↑	The state of	== 3:0V=	10↑			ns
Data Hold Time, T <sub>H</sub>		41	Total Lines		01		a to me a	ns

The (1) arrow indicates the positive edge of the Clock is used for reference.

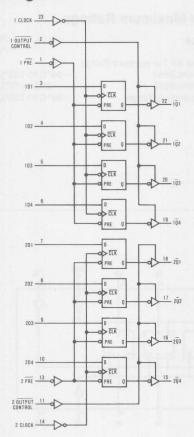
	Parameter	Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Voltage	V <sub>CC</sub> = 4.5V I <sub>I</sub> =	-18mA			-1.5	V
Vон	High Level Output Voltage	$V_{CC} = 4.5V$ $V_{IL} = V_{IL} MAX$	54/74ALS I <sub>OH</sub> = -1mA	2.4	3.2		٧
	80		74ALS I <sub>OH</sub> = -2.6mA	2.4	3.3		٧
	Tea Total	$I_{OH} = -400\mu A$	54/74ALS	V <sub>CC</sub> -2		9019	V
VOL	Low Level Output Voltage	V <sub>CC</sub> = 4.5V V <sub>IH</sub> = 2V	54/74ALS I <sub>OL</sub> = 12mA	RE PRE	0.25	0.4	V
			74ALS I <sub>OL</sub> = 24mA		0.35	0.5	V
lį	Max High Input Current	$V_{CC} = 5.5V V_{IH}$	= 7V			0.1	mA
IIH	High Level Input Current	$V_{CC} = 5.5V V_{IH}$	= 2.7V			20	μΑ
IIL	Low Level Input Current	V <sub>CC</sub> = 5.5V V <sub>IL</sub>	= 0.4V			-0.2	mA
IO	Output Drive Current	$V_{CC} = 5.5V$	54/74ALS V <sub>O</sub> = 2.25V	-30		-110	mA
lozh	Off-State Output Current, High Level Voltage Applied	$V_{CC} = 5.5V V_{IH}$ $V_{O} = 2.7V$	= 2V		ragilean i	20	μΑ
lozL	Off-State Output Current, Low Level Voltage Applied	$V_{CC} = 5.5V V_{IH}$ $V_{O} = 0.4V$	= 2V			-20	μΑ
Icc	Supply Current	V <sub>CC</sub> = 5.5V	Outputs High		14	21	mA
		Outputs Open	Outputs Low		18	29	mA
			Outputs Disabled		20	31	mA

#### Switching Characteristics over recommended operating free air temperature range (Note 1)

				DI	DM54ALS876			M74ALS8	76	11
Parameter	From	То	Conditions	Min	Тур	Max	Min	Тур	Max	Unit
FMAX				30			35			MH
TPLH	Clock	Any Q		4		15	4		12	ns
TPHL	Olook	,, c		4		15	4		12	ns
T <sub>PZH</sub>	Output	Any Q	$V_{CC} = 4.5V \text{ to } 5.5V$ $R_L = 500 \Omega$	4		21	4	Del	18	ns
TPZL	Control	7 m y Q	$C_L = 50 \text{ pF}$	4		21	4		18	ns
TPHZ		30,02164	ncassill back grandillib!	2	inches (	10	2	Grafamen	8	ns
TPLZ	That medicate	and the same	Breming Specimens	3		15	3		13	ns
TPHL	Preset	Any Q		6	a Travella	22	6	na Spiri	19	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-5.

#### **Logic Diagram**



#### **Function Table**

PRE	D	CLK	OC	Q
X	X	X	Н	Z
L	X	X	L	L
Н	Н	1	L	L
Н	L	1	L	Н
Н	X	L	L	Qo



# DM54ALS880/DM74ALS880 Dual 4-Bit D-Type Transparent Latches With Inverted Outputs

#### **General Description**

These Dual 4-Bit inverting registers feature totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight inverting latches of the ALS880 are transparent D-type latches meaning that while the enable (G) is high the  $\overline{Q}$  outputs will follow the complement of the data (D) inputs. When the enable is taken low the output will be latched at the complement of the level of the data that was set up.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches. That is, the old data can be retained or new data can be entered even while the outputs are off.

#### **Features**

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- 3-State Buffer-Type Outputs Drive Bus Lines Directly.
- Space Saving 300 Mil Wide Package.

#### **Absolute Maximum Ratings**

 Supply Voltage
 7V

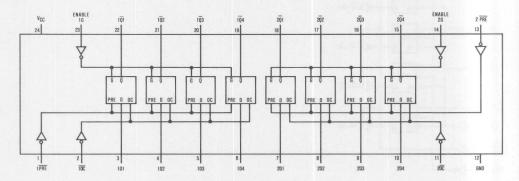
 Input Voltage
 7V

 Operating Free Air Temperature Range
 -55°C to 125°C

 DM54ALS880
 -55°C to 70°C

 Storage Temperature Range
 -65°C to 150°C

#### **Connection Diagram**



54ALS880 (J) 74ALS880 (J,N)

	0	M54ALS8	80	D	M74ALS8	30	Unit
Parameter	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, VCC	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, VIH	2			2		MENTAL STATE	V
Low Level Input Voltage, VIL	amile - Taro		0.8			0.8	V
High Level Output Voltage, VOH	B ARAL	Autor	5.5			5.5	V
High Level Output Current, IOH			-1.0		MAN COMP	-2.6	mA
Low Level Output Current, IOL			12			24	mA
Pulse Width, T <sub>W</sub> Enable Preset Low	15 15	and Med	-	15 15	la overel de	Pl mokil	ns ns
Data Setup Time, TSU	18↓	W Val	- 307	15↓	term lies	u dele	ns
Data Hold Time, T <sub>H</sub>	0↓	i ik va	W nest	0↓	Manual Face	J wed	ns

The  $(\downarrow)$  arrow indicates the negative edge of the enable is used for reference.

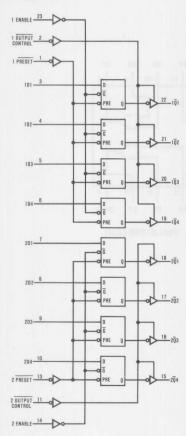
	Parameter	Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Voltage	V <sub>CC</sub> = 4.5V I <sub>I</sub> =	-18mA			-1.5	٧
Vон	High Level Output Voltage	V <sub>CC</sub> = 4.5V V <sub>IL</sub> = V <sub>IL</sub> MAX	54/74ALS I <sub>OH</sub> = -1mA	2.4	3.2		٧
	20		$74ALS$ $I_{OH} = -2.6mA$	2.4	3.3		٧
		$I_{OH} = -400\mu A$	54/74ALS	V <sub>CC</sub> -2			٧
VOL	Low Level Output Voltage	V <sub>CC</sub> = 4.5V V <sub>IH</sub> = 2V	54/74ALS I <sub>OL</sub> = 12mA		0.25	0.4	٧
			74ALS I <sub>OL</sub> = 24mA		0.35	0.5	٧
l <sub>l</sub>	Max High Input Current	$V_{CC} = 5.5V V_{IH}$	= 7V		en allo	0.1	mA
IH	High Level Input Current	$V_{CC} = 5.5V V_{IH}$	= 2.7V			20	μΑ
IIL	Low Level Input Current	$V_{CC} = 5.5V V_{IL}$	= 0.4V			-0.2	mA
IO	Output Drive Current	$V_{CC} = 5.5V$	54/74ALS V <sub>O</sub> = 2.25V	-30		-110	mA
lozh	Off-State Output Current, High Level Voltage Applied	$V_{CC} = 5.5V V_{IH}$ $V_{O} = 2.7V$	= 2V			20	μΑ
lozL	Off-State Output Current, Low Level Voltage Applied	$V_{CC} = 5.5V V_{IH}$ $V_{O} = 0.4V$	= 2V			-20	μΑ
ICC	Supply Current	V <sub>CC</sub> = 5.5V	Outputs High		14	21	mA
		Outputs Open	Outputs Low		19	29	mA
			Outputs Disabled		20	31	m.A

Switching Characteristics over recommended operating free air temperature range (Note 1)

				DI	M54ALS8	80	DN	M74ALS8	380	
Parameter	From	То	Conditions	Min	Тур	Max	Min	Тур	Max	Unit
TPLH	Data	Any Q		3		23	3	ARA-	20	ns
T <sub>PHL</sub>		7 mily Ca		3		15	3		12	ns
TPLH	Enable	Any Q	$V_{CC} = 4.5V \text{ to } 5.5V$	8		31	8		24	ns
T <sub>PHL</sub>	Lilabio	7 tily G	$R_{L} = 500 \Omega$ $C_{L} = 50 \text{ pF}$	8		22	8	1.3.	21	ns
TPZH	200		- OL 00 pi	4		21	5		18	ns
TPZL	Output	Any Q	minimize scientific	4		21	5	Manh	18	ns
TPHZ	Control	7.1.1, 0	pouriov suspin	2		10	2		8	ns
TPLZ	200		DESTRUMBATION .	3		15	3	della co	13	ns
TPHL	Preset	Any Q	MOTO MANAGEMENT OF THE PARTY OF	6		24	6		21	ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-5.

#### **Logic Diagram**



#### **Function Table**

PRE	D	EN	OC	Q
X	X	X	Н	Z
L	X	X	L	L
Н	Н	Н	L	L
Н	L	Н	L	Н
Н	X	L	L	Q

National Semiconductor

Preliminary

# DM54ALS1000/DM74ALS1000 Quadruple 2-Input NAND Buffers

#### **Features**

#### **Absolute Maximum Ratings**

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Improved Line Receiving Characteristics.

Supply Voltage Input Voltage

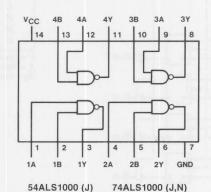
Operating Free Air Temperature Range DM54ALS1000

DM74ALS1000 Storage Temperature Range 7V 7V

-55°C to 125°C 0°C to 70°C -65°C to 150°C

#### **Connection Diagram**

 $Y = \overline{AB}$ 



	D	M54ALS10	000	D	000		
Parameter	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, VCC	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, VIH	2	10/1-9	Milita	2	2-1	elqin	V
Low Level Input Voltage, VIL			0.8			0.8	V
High Level Output Current, IOH			-1.0			-2.6	mA
Low Level Output Current, IOL	Convey 4		12		u 2 maile	24	mA

# Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Тур	Max	Uni
VIK	Input Clamp Voltage	$V_{CC} = 4.5 V I_{I} = -$	18mA			-1.5	٧
Vон	High Level Output Voltage	$V_{CC} = 4.5V$ $V_{IL} = V_{IL} MAX$	54/74ALS I <sub>OH</sub> = -1mA	2.4	3.2		٧
			74ALS I <sub>OH</sub> = -2.6mA	2.4	3.3		V
		$I_{OH} = -400\mu A$	54/74ALS	V <sub>CC</sub> -2			V
VOL	Low Level Output Voltage	$V_{CC} = 4.5V$ $V_{IH} = 2V$	54/74ALS I <sub>OL</sub> = 12mA		0.25	0.4	٧
			74ALS I <sub>OL</sub> = 24mA		0.35	0.5	٧
lμ	Max High Input Current	V <sub>CC</sub> = 5.5V V <sub>IH</sub> =	7V			0.1	mA
lін	High Level Input Current	V <sub>CC</sub> = 5.5V V <sub>IH</sub> =	2.7V			20	μΑ
IIL	Low Level Input Current	V <sub>CC</sub> = 5.5V V <sub>IL</sub> =	0.4V			-0.2	mA
10	Output Drive Current	$V_{CC} = 5.5V$	$V_{O} = 2.25V$	-30		-110	mA
Іссн	Supply Current	Outputs High VCC	= 5.5V, VI = 0V		0.86	1.6	mA
ICCL	Supply Current	Outputs Low VCC	= 5.5V, VI = 4.5V		4.0	6.4	mA

# Switching Characteristics over recommended operating free air temperature range (Note 1)

		Di	M54ALS10	000	DI	M74ALS10	000	
Parameter	Conditions	Min	Тур	Max	Min	Тур	Max	Unit
TPLH, Propagation delay time. Low to high Level Output	$V_{CC} = 4.5 \text{ to } 5.5V$ $R_L = 500  \Omega,$ $C_L = 50  \text{pF}.$	2		10	2		8	ns
TPHL, Propagation delay time. High to low Level Output		3		10	3		8	ns

# DM54ALS1002/DM74ALS1002 Quadruple 2-Input Positive-Nor Buffers

#### **Features**

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and VCC Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Improved Line Receiving Characteristics.

#### **Absolute Maximum Ratings**

Supply Voltage Input Voltage Operating Free Air Temperature Range DM54ALS1002

-55°C to 125°C 0°C to 70°C

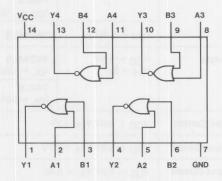
DM74ALS1002 Storage Temperature Range

-65°C to 150°C

7V 7V

# **Connection Diagram**

Y = A + B



54ALS1002 (J) 74ALS1002 (J,N)

	DI	M54ALS10	002	D	M74ALS10	02	
Parameter	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, V <sub>CC</sub>	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, VIH	2		ONA	2	eni-t		V
Low Level Input Voltage, VIL			0.8	10/10	alle D	0.8	V
High Level Output Current, IOH			-1.0			-2.6	mA
Low Level Output Current, IOL	Turnilla viorial		12	H Nat		24	mA

#### **Electrical Characteristics** over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Voltage	$V_{CC} = 4.5 V I_{I} = -$	-18mA			-1.5	V
Vон	High Level Output Voltage	$V_{CC} = 4.5V$ $V_{IL} = V_{IL} MAX$	54/74ALS I <sub>OH</sub> = -1mA	2.4	3.2		V
			$74ALS$ $I_{OH} = -2.6mA$	2.4	3.3	E dens	V
		$I_{OH} = -400\mu A$	54/74ALS	V <sub>CC</sub> -2			V
VOL	Low Level Output Voltage	$V_{CC} = 4.5V$ $V_{IH} = 2V$	54/74ALS I <sub>OL</sub> = 12mA		0.25	0.4	V
			74ALS I <sub>OL</sub> = 24mA		0.35	0.5	V
lj .	Max High Input Current	V <sub>CC</sub> = 5.5V V <sub>IH</sub> =	7V			0.1	mA
ΙΗ	High Level Input Current	V <sub>CC</sub> = 5.5V V <sub>IH</sub> =	2.7V	135-5		20	μΑ
IIL	Low Level Input Current	$V_{CC} = 5.5V V_{IL} =$	0.4V			-0.2	mA
IO	Output Drive Current	$V_{CC} = 5.5V$	V <sub>O</sub> = 2.25V	-30		-110	mA
ІССН	Supply Current	Outputs High VCC	; = 5.5V, VI = 0V		1.7	2.8	mA
ICCL	Supply Current	Outputs Low VCC	= 5.5V, VI = 4.5V		4.8	8.0	mA

# Switching Characteristics over recommended operating free air temperature range (Note 1)

		DM54ALS1002			DI			
Parameter	Conditions	Min	Тур	Max	Min	Тур	Max	Unit
TPLH, Propagation delay time. Low to high Level Output	$V_{CC} = 4.5 \text{ to } 5.5V$ $R_L = 500 \Omega,$ $C_L = 50 \text{pF}.$	2		10	2		8	ns
TPHL, Propagation delay time. High to low Level Output		3		10	3		8	ns

# DM54ALS1003/DM74ALS1003 Quadruple 2-Input NAND Buffers with Open-Collector Outputs

#### **Features**

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with LS TTL Counterpart.
- Improved Line Receiving Characteristics.

#### **Absolute Maximum Ratings**

Supply Voltage Input Voltage Off State (High Level) Output Voltage Operating Free Air Temperature Range DM54ALS1003

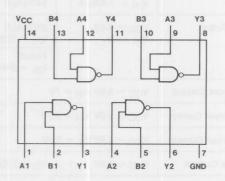
DM54ALS1003 DM74ALS1003 Storage Temperature Range -55°C to 125°C 0°C to 70°C -65°C to 150°C

7V 7V

7V

#### **Connection Diagram**

 $Y = \overline{AB}$ 



54ALS1003 (J) 74ALS1003 (J,N)

	DI	M54ALS10	03	DI			
Parameter	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, VCC	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, VIH	2			2			V
Low Level Input Voltage, VIL			0.8			0.8	V
High Level Output Voltage, VOH			5.5	a Grand was		5.5	V
Low Level Output Current, IOL	Liv. Alekei		12		A Lewise	24	mA

#### Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Voltage	V <sub>CC</sub> = 4.5V I <sub>I</sub> =	-18mA			-1.5	V
ГОН	High Level Output Current	$V_{CC} = 4.5V$ $V_{OH} = 5.5V$			insgn)	100	μΑ
VOL	Low Level Output Voltage	$V_{CC} = 4.5V$ $V_{IH} = 2V$	54/74ALS I <sub>OL</sub> = 12mA		0.25	0.4	V
			74ALS I <sub>OL</sub> = 24mA		0.35	0.5	V
lį	Max High Input Current	V <sub>CC</sub> = 5.5V V <sub>IH</sub>	= 7V			0.1	mA
IIH	High Level Input Current	V <sub>CC</sub> = 5.5V V <sub>IH</sub>	= 2.7V			20	μΑ
I <sub>I</sub> L	Low Level Input Current	V <sub>CC</sub> = 5.5V V <sub>IL</sub>	= 0.4V			-0.2	mA
IO	Output Drive Current	$V_{CC} = 5.5V$	$V_{O} = 2.25V$	-30		110	mA
ІССН	Supply Current	Outputs High Vo	CC = 5.5V, VI = 0V		0.86	1.6	mA
ICCL	Supply Current	Outputs Low Vo	CC = 5.5V, VI = 4.5V		4.0	6.4	mA

# Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter		DM54ALS1003			DI			
	Conditions	Min	Тур	Max	Min	Тур	Max	Unit
TPLH, Propagation delay time. Low to high Level Output	$V_{CC} = 4.5 \text{ to } 5.5V$ $R_L = 667 \Omega$ , $C_L = 50 \text{ pF}$ .	10		40	10		30	ns
TPHL, Propagation delay time. High to low Level Output		7		18	7		15	ns

National Semiconductor

Preliminary

# DM54ALS1004/DM74ALS1004 Hex Inverting Drivers

#### **Features**

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin for Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

#### **Absolute Maximum Ratings**

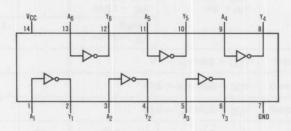
Supply Voltage 7V
Input Voltage 7V
Operating Free Air Temperature Range
DM54ALS -55°C to 125°C

DM54ALS —55°C to 125°C

DM74ALS 0°C to 70°C

Storage Temperature Range —65°C to 150°C

#### **Connection Diagram**



54ALS1004 (J) 74ALS1004 (J,N)

	D	M54ALS10	004	DI	04		
Parameter	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, VCC	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, VIH	2		Hillar.	2	plied		V
Low Level Input Voltage, V <sub>IL</sub>			0.8			0.8	V
High Level Output Current, IOH			-1.0			-2.6	mA
Low Level Output Current, IOL			12			24	mA

# Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Тур	Max	Uni
VIK	Input Clamp Voltage	$V_{CC} = 4.5V, I_{I} =$	-18mA		and a line	-1.5	V
Vон	High Level Output	$I_{OH} = -0.4$ mA		V <sub>CC</sub> -2			V
	Voltage	I <sub>OH</sub> = MAX		2.4		d nod	V
VOL	Low Level Output Voltage	V <sub>CC</sub> = 4.5V	54/74ALS I <sub>OL</sub> = 12mA		0.25	0.4	V
			74 ALS I <sub>OL</sub> = 24mA		0.35	0.5	V
lı	Max High Input Current	V <sub>CC</sub> = 5.5V, V <sub>IH</sub>	= 7V			0.1	mA
lін	High Level Input Current	$V_{CC} = 5.5V, V_{IH}$	= 2.7V	-		20	μΑ
IIL	Low Level Input Current	$V_{CC} = 5.5V, V_{IL}$	= 0.4V			-0.2	mA
Ю	Output Drive Current	V <sub>CC</sub> = 5.5V	$V_0 = 2.25V$	-30		-110	mA
Icc	Supply Current	$V_{CC} = 5.5V$	Outputs High		0.14		m/
			Outputs Low		1.2		m.A

# Switching Characteristics over recommended operating free air temperature range (Note 1)

		DM54ALS1004			DI			
Parameter	Conditions	Min	Тур	Max	Min	Тур	Max	Uni
TPLH, Propagation delay time. Low to high Level Output	$V_{CC} = 4.5 \text{ to } 5.5V$ $R_L = 500 \Omega,$ $C_L = 50 \text{pF}.$	1.4	2.8	7.5	1.4	2.8	6.0	ns
TPHL, Propagation delay time. High to low Level Output		1.2	2.4	6.5	1.2	2.4	5.0	ns

7V 7V

-65°C to 150°C

#### **Features**

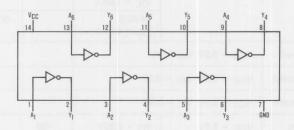
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and VCC Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL
- Functionally and Pin for Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

#### **Absolute Maximum Ratings**

Storage Temperature Range

Supply Voltage Input Voltage Operating Free Air Temperature Range DM54ALS -55°C to 125°C 0°C to 70°C DM74ALS

**Connection Diagram** 



54ALS1005 (J) 74ALS1005 (J,N)

	D	M54ALS10	05	D			
Parameter	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, VCC	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, VIH	2			2	gall-X		V
Low Level Input Voltage, VIL			0.8			0.8	V
High Level Output Voltage, VOH			5.5			5.5	V
Low Level Output Current, IOL			12			24	mA

#### **Electrical Characteristics** over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Voltage	$V_{CC} = 4.5V, I_{I} =$	-18mA			-1.5	V
ЮН	High Level Output Current	$V_{CC} = 4.5V, V_{OP}$	H = 5.5V			100	μΑ
VOL	Low Level Output Voltage	$V_{CC} = 4.5V$	54/74ALS I <sub>OL</sub> = 12mA		0.25	0.4	V
			74 ALS I <sub>OL</sub> = 24mA		0.35	0.5	V
l <sub>l</sub>	Max High Input Current	V <sub>CC</sub> = 5.5V, V <sub>IH</sub>	= 7V		ill = x	0.1	mA
ΙΗ	High Level Input Current	$V_{CC} = 5.5V, V_{IH}$	= 2.7V			20	μΑ
I <sub>I</sub> L	Low Level Input Current	$V_{CC} = 5.5V, V_{IL}$	= 0.4V			-0.2	mA
ICC	Supply Current	$V_{CC} = 5.5V$	Outputs High		0.14		mA
			Outputs Low		1.2		mA

# Switching Characteristics over recommended operating free air temperature range (Note 1)

		DM54ALS1005			DI	I I I I I		
delay time. Low to	Conditions	Min	Тур	Max	Min	Тур	Max	Unit
TPLH, Propagation delay time. Low to high Level Output	$V_{CC} = 4.5 \text{ to } 5.5V$ $R_L = 667 \Omega$ , $C_L = 50 \text{ pF}$ .	7	10	25	7	10	20	ns
TPHL, Propagation delay time. High to low Level Output		1.2	3	6.5	1.2	3	5	ns

# DM54ALS1008/DM74ALS1008 Quadruple 2-Input AND Buffers

#### **Features**

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Improved Line Receiving Characteristics.

#### **Absolute Maximum Ratings**

Supply Voltage Input Voltage Operating Free Air Temperature Range

DM54ALS1008 DM74ALS1008 -55°C to 125°C 0°C to 70°C -65°C to 150°C

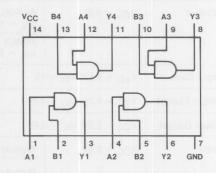
7V

7V

Storage Temperature Range

# **Connection Diagram**

Y = AR



54ALS1008 (J) 74ALS1008 (J,N)

	D	M54ALS10	800	DI	08		
Parameter	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, VCC	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, VIH	2			2			٧
Low Level Input Voltage, VIL	eld studen		0.8			0.8	V
High Level Output Current, IOH			-1.0		7 10 100	-2.6	mA
Low Level Output Current, IOL			12			24	mA

#### **Electrical Characteristics** over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Voltage	$V_{CC} = 4.5V I_{I} = -$	-18mA			-1.5	V
Vон	High Level Output Voltage	$V_{CC} = 4.5V$ $V_{IH} = 2V$	54/74ALS I <sub>OH</sub> = -1mA	2.4	3.2		V
		101 105 47 11 101 101 101 20	74ALS I <sub>OH</sub> = -2.6mA	2.4	3.3		٧
		$I_{OH} = -400\mu A$	54/74ALS	V <sub>CC</sub> -2			٧
VOL	Low Level Output Voltage	$V_{CC} = 4.5V$ $V_{IL} = .8V$	54/74ALS I <sub>OL</sub> = 12mA		0.25	0.4	V
			74ALS I <sub>OL</sub> = 24mA		0.35	0.5	V
lį	Max High Input Current	V <sub>CC</sub> = 5.5V V <sub>IH</sub> =	7V			0.1	mA
ΊΗ	High Level Input Current	V <sub>CC</sub> = 5.5V V <sub>IH</sub> =	2.7V			20	μΑ
IIL	Low Level Input Current	$V_{CC} = 5.5 \dot{V} V_{IL} =$	0.4V			-0.2	mA
10	Output Drive Current	$V_{CC} = 5.5V$	$V_{O} = 2.25V$	-30		-110	mA
Іссн	Supply Current	Outputs High VCC	; = 5.5V, VI = 4.5V		1.7	2.8	mA
ICCL	Supply Current	Outputs Low VCC	= 5.5V, VI = 0V		4.8	8.0	mA

# Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter		DM54ALS1008			DI			
	Conditions	Min	Тур	Max	Min	Тур	Max	Unit
TPLH, Propagation delay time. Low to high Level Output	$V_{CC} = 4.5 \text{ to } 5.5V$ $R_L = 500  \Omega,$ $C_L = 50  \text{pF}.$	3		12	3		10	ns
TPHL, Propagation delay time. High to low Level Output		4		12	4		10	ns

# DM54ALS1010/DM74ALS1010 Triple 3-Input NAND Buffers

#### **Features**

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Improved Line Receiving Characteristics.

#### **Absolute Maximum Ratings**

Supply Voltage Input Voltage Operating Free Air Temperature Range

Storage Temperature Range

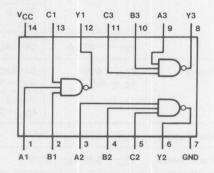
0°C to 70°C -65°C to 150°C

7V

7V

#### **Connection Diagram**

 $Y = \overline{ABC}$ 



54ALS1010 (J)

74ALS1010 (J,N)

	D	M54ALS10	010	D	10		
Parameter	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, VCC	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, VIH	2		19070	2			٧
Low Level Input Voltage, VIL			0.8			0.8	V
High Level Output Current, IOH			-1.0		E ra a sonin	-2.6	mA
Low Level Output Current, IOL	ng may hav		12	S Legend		24	mA

#### Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Тур	Max	Uni
VIK	Input Clamp Voltage	V <sub>CC</sub> = 4.5V I <sub>I</sub> = -	-18mA			-1.5	V
VOH	High Level Output Voltage	$V_{CC} = 4.5V$ $V_{IL} = V_{IL} MAX$	54/74ALS I <sub>OH</sub> = -1mA	2.4	3.2		٧
	27 48	a -a- a a	74ALS I <sub>OH</sub> = -2.6mA	2.4	3.3		V
		$I_{OH} = -400\mu A$	54/74ALS	V <sub>CC</sub> -2			V
VOL	Low Level Output Voltage	$V_{CC} = 4.5V$ $V_{IH} = 2V$	54/74ALS I <sub>OL</sub> = 12mA		0.25	0.4	٧
			74ALS I <sub>OL</sub> = 24mA		0.35	0.5	V
lį	Max High Input Current	V <sub>CC</sub> = 5.5V V <sub>IH</sub> =	: 7V			0.1	mA
ΙΗ	High Level Input Current	V <sub>CC</sub> = 5.5V V <sub>IH</sub> =	2.7V			20	μΑ
IIL	Low Level Input Current	$V_{CC} = 5.5V V_{IL} =$	0.4V			-0.2	mA
10	Output Drive Current	$V_{CC} = 5.5V$	$V_{O} = 2.25V$	-30		-110	mA
ІССН	Supply Current	Outputs High VCC	; = 5.5V, VI = 0V		0.65	1.1	mA
ICCL	Supply Current	Outputs Low VCC	= 5.5V, VI = 4.5V		3.1	5.0	mA

#### Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter		DM54ALS1010			DI			
	Conditions	Min	Тур	Max	Min	Тур	Max	Unit
TPLH, Propagation delay time. Low to high Level Output	$V_{CC} = 4.5 \text{ to } 5.5V$ $R_L = 500 \Omega,$ $C_L = 50 \text{pF}.$	2		11	2		9	ns
TPHL, Propagation delay time. High to low Level Output		3		11	3		9	ns

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# DM54ALS1011/DM74ALS1011 Triple 3-Input AND Buffers

#### **Features**

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Improved Line Receiving Characteristics.

#### **Absolute Maximum Ratings**

Supply Voltage Input Voltage

Operating Free Air Temperature Range

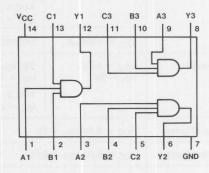
DM54ALS1011 DM74ALS1011 Storage Temperature Range -55°C to 125°C 0°C to 70°C

7V 7V

-65°C to 150°C

#### **Connection Diagram**

Y = ABC



	DI	M54ALS10	111	D	11	11-24	
Parameter	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, VCC	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, VIH	2		reth	2	AM B		V
Low Level Input Voltage, VIL			0.8			0.8	V
High Level Output Current, IOH			-1.0			-2.6	mA
Low Level Output Current, IOL			12	G lakini	Est Ente	24	mA

#### Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Voltage	$V_{CC} = 4.5 V I_{I} = -$	$V_{CC} = 4.5 V I_I = -18 \text{mA}$			-1.5	V
VOH	High Level Output Voltage	V <sub>CC</sub> = 4.5V V <sub>IH</sub> = 2V	54/74ALS I <sub>OH</sub> = -1mA	2.4	3.2		V
			$74ALS$ $I_{OH} = -2.6mA$	2.4	3.3		V
		$I_{OH} = -400\mu A$	54/74ALS	V <sub>CC</sub> -2			V
VOL	Low Level Output Voltage	$V_{CC} = 4.5V$ $V_{IL} = .8V$	54/74ALS I <sub>OL</sub> = 12mA		0.25	0.4	٧
			74ALS I <sub>OL</sub> = 24mA		0.35	0.5	V
lį	Max High Input Current	V <sub>CC</sub> = 5.5V V <sub>IH</sub> =	7V			0.1	mA
lін	High Level Input Current	V <sub>CC</sub> = 5.5V V <sub>IH</sub> =	2.7V			20	μΑ
IIL	Low Level Input Current	$V_{CC} = 5.5V V_{IL} =$	0.4V			-0.2	mA
Io	Output Drive Current	$V_{CC} = 5.5V$	$V_{O} = 2.25V$	-30		-110	mA
ІССН	Supply Current	Outputs High VCC	; = 5.5V, VI = 4.5V		1.2	2.0	m.A
ICCL	Supply Current	Outputs Low VCC	= 5.5V, VI = 0V		3.6	5.8	m/

# Switching Characteristics over recommended operating free air temperature range (Note 1)

		DM54ALS1011			DI			
delay time. Low to	Conditions	Min	Тур	Max	Min	Тур	Max	Unit
TPLH, Propagation delay time. Low to high Level Output	$V_{CC} = 4.5 \text{ to } 5.5V$ $R_L = 500 \Omega,$ $C_L = 50 \text{pF}.$	3		13	3		11	ns
TPHL, Propagation delay time. High to low Level Output		4		13	4		11	ns

# DM54ALS1020/DM74ALS1020 Dual 4-Input NAND Buffers

#### **Features**

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Improved Line Receiving Characteristics.

#### **Absolute Maximum Ratings**

Supply Voltage
Input Voltage
Operating Free Air Temperature Range
DM54ALS1020
DM74ALS1020

-55°C to 125°C 0°C to 70°C -65°C to 150°C

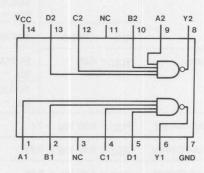
7V

7V

Storage Temperature Range

#### **Connection Diagram**

 $Y = \overline{ABCD}$ 



54ALS1020 (J) 74ALS1020 (J,N)

	D	M54ALS10	020	D			
Parameter	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, V <sub>CC</sub>	4.5	5	5.5	4.5	5	5.5	٧
High Level Input Voltage, VIH	2	and the	Tues I	2	ant-C		٧
Low Level Input Voltage, VIL			0.8			0.8	V
High Level Output Current, IOH			-1.0			-2.6	mA
Low Level Output Current, IOL			12	O heaving	14.6 mg/	24	mA

# Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Voltage	V <sub>CC</sub> = 4.5V I <sub>I</sub> = -	-18mA			-1.5	V
VOH	High Level Output Voltage	$V_{CC} = 4.5V$ $V_{IL} = V_{IL} MAX$	54/74ALS I <sub>OH</sub> = -1mA	2.4	3.2		٧
	100 mg	S = 10 H	$74ALS$ $I_{OH} = -2.6mA$	2.4	3.3		٧
		$I_{OH} = -400\mu A$	54/74ALS	V <sub>CC</sub> -2			V
VOL	Low Level Output Voltage	$V_{CC} = 4.5V$ $V_{IH} = 2V$	54/74ALS I <sub>OL</sub> = 12mA		0.25	0.4	٧
		IT C	74ALS I <sub>OL</sub> = 24mA		0.35	0.5	٧
h	Max High Input Current	V <sub>CC</sub> = 5.5V V <sub>IH</sub> =	7V			0.1	mA
ΊΗ	High Level Input Current	V <sub>CC</sub> = 5.5V V <sub>IH</sub> =	2.7V			20	μΑ
IIL	Low Level Input Current	$V_{CC} = 5.5V V_{IL} =$	0.4V			-0.2	mA
10	Output Drive Current	$V_{CC} = 5.5V$	$V_0 = 2.25V$	-30		-110	mA
Іссн	Supply Current	Outputs High VCC	; = 5.5V, VI = 0V		0.43	0.8	mA
ICCL	Supply Current	Outputs Low VCC	= 5.5V, VI = 4.5V		2.0	3.2	mA

# Switching Characteristics over recommended operating free air temperature range (Note 1)

Danamatan		DM54ALS1020			DI			
Parameter	Conditions	Min	Тур	Max	Min	Тур	Max	Unit
TPLH, Propagation delay time. Low to high Level Output	$V_{CC} = 4.5 \text{ to } 5.5V$ $R_L = 500 \Omega,$ $C_L = 50 \text{pF}.$	2		10	2		8	ns
TPHL, Propagation delay time. High to low Level Output		3		10	3		8	ns

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# DM54ALS1032/DM74ALS1032 Quadruple 2-Input OR Buffers

#### **Features**

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Improved Line Receiving Characteristics.

#### **Absolute Maximum Ratings**

Supply Voltage
Input Voltage

Operating Free Air Temperature Range DM54ALS1032 DM74ALS1032

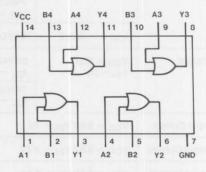
Storage Temperature Range

7V 7V

-55°C to 125°C 0°C to 70°C -65°C to 150°C

#### **Connection Diagram**

Y = A + B



54ALS1032 (J) 74ALS1032 (J,N)

	Di	M54ALS10	32	DI	32		
Parameter	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, VCC	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, VIH	2			2			V
Low Level Input Voltage, VIL			0.8			0.8	V
High Level Output Current, IOH	ou dor stor		-1.0	Daniel se		-2.6	mA
Low Level Output Current, IOL	Nation I		12	de l'errie		24	mA

#### Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Voltage	$V_{CC} = 4.5 V I_{I} = -$	-18mA			-1.5	V
Vон	High Level Output Voltage	$V_{CC} = 4.5V$ $V_{IH} = 2V$	54/74ALS I <sub>OH</sub> = -1mA	2.4	3.2	O soit	V
			$74ALS$ $I_{OH} = -2.6mA$	2.4	3.3		V
		$I_{OH} = -400\mu A$	54/74ALS	V <sub>CC</sub> -2			V
VOL	Low Level Output Voltage	$V_{CC} = 4.5V$ $V_{IH} = .8V$	54/74ALS I <sub>OL</sub> = 12mA		0.25	0.4	٧
			74ALS I <sub>OL</sub> = 24mA		0.35	0.5	V
lį	Max High Input Current	V <sub>CC</sub> = 5.5V V <sub>IH</sub> =	7V			0.1	mA
Ιн	High Level Input Current	$V_{CC} = 5.5V V_{IH} =$	2.7V			20	μΑ
IIL	Low Level Input Current	$V_{CC} = 5.5V V_{IL} =$	0.4V			-0.2	mA
10	Output Drive Current	$V_{CC} = 5.5V$	$V_{O} = 2.25V$	-30		-110	mA
Іссн	Supply Current	Outputs High VCC	; = 5.5V, VI = 4.5V		2.3	4.0	mA
ICCL	Supply Current	Outputs Low VCC	= 5.5V, VI = 0V		5.6	9.1	mA

#### Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter		DI	M54ALS10	32	DI	M74ALS10	32	
	Conditions	Min	Тур	Max	Min	Тур	Max	Unit
T <sub>PLH</sub> , Propagation delay time. Low to high Level Output	$V_{CC} = 4.5 \text{ to } 5.5V$ $R_L = 500 \Omega$ , $C_L = 50 \text{ pF}$ .	3		12	3		10	ns
TPHL, Propagation delay time. High to low Level Output		4		12	4		10	ns

Preliminary

-65°C to 150°C

# DM54ALS1034/DM74ALS1034 Hex Non-Inverting Drivers

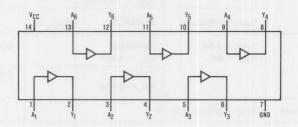
#### **Features**

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and VCC Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL
- Functionally and Pin for Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

#### **Absolute Maximum Ratings**

Supply Voltage 7V Input Voltage 7V Operating Free Air Temperature Range DM54ALS -55°C to 125°C DM74ALS 0°C to 70°C Storage Temperature Range

#### **Connection Diagram**



74ALS1034 (J,N) 54ALS1034 (J)

	D	DM54ALS1034 DM74ALS1034				34	
Parameter	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, VCC	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, VIH	2	1	ignuc	2	ellos	rearg!	٧
Low Level Input Voltage, VIL			0.8			0.8	٧
High Level Output Current, IOH	5117 - a t (12.m.3)		-1.0			-2.6	mA
Low Level Output Current, IOL			12	li hepitar		24	mA

#### Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Тур	Max	Uni
VIK	Input Clamp Voltage	V <sub>CC</sub> = 4.5V, I <sub>I</sub> =	$V_{CC} = 4.5V, I_{I} = -18mA$		- Piname	-1.5	٧
Vон	High Level Output	$I_{OH} = -0.4$ mA		V <sub>CC</sub> -2			V
	Voltage	I <sub>OH</sub> = MAX		2.4		3.0002	V
VOL	Low Level Output Voltage	V <sub>CC</sub> = 4.5V	54/74ALS I <sub>OL</sub> = 12mA		0.25	0.4	V
			74 ALS I <sub>OL</sub> = 24mA		0.35	0.5	V
l <sub>I</sub>	Max High Input Current	$V_{CC} = 5.5V, V_{IH}$	= 7V			0.1	mA
lіН	High Level Input Current	$V_{CC} = 5.5V, V_{IH}$	= 2.7V			20	μΑ
I <sub>I</sub> L	Low Level Input Current	$V_{CC} = 5.5V, V_{IL}$	= 0.4V			-0.2	mA
10	Output Drive Current	$V_{CC} = 5.5V$	V <sub>O</sub> = 2.25V	-30		-110	mA
Icc	Supply Current	$V_{CC} = 5.5V$	Outputs High		0.53		mA
			Outputs Low		1.3		mA

#### Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter		DI	M54ALS10	34	DM74ALS1034			
	Conditions	Min	Тур	Max	Min	Тур	Max	Unit
TPLH, Propagation delay time. Low to high Level Output	$V_{CC} = 4.5 \text{ to } 5.5 \text{V}$ $R_L = 500 \Omega,$ $C_L = 50  \text{pF}.$	1.8	4.0	10	2.2	4.5	9	ns
TPHL, Propagation delay time. High to low Level Output		2.2	4.5	12	2.2	4.5	9	ns

65°C to 150°C

# DM54ALS1035/DM74ALS1035 Hex Non-Inverting Drivers with Open Collector Outputs

#### **Features**

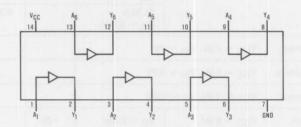
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V<sub>CC</sub> Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin for Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

#### **Absolute Maximum Ratings**

Supply Voltage 7V
Input Voltage 7V
Operating Free Air Temperature Range
DM54ALS -55°C to 125°C
DM74ALS 0°C to 70°C

Storage Temperature Range

#### **Connection Diagram**



54ALS1035 (J) 74ALS1035 (J,N)

	Di	DM54ALS1035 DM74ALS				35	
Parameter	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, VCC	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, VIH	2	llase.	a) ens	2	eus •	ata	V
Low Level Input Voltage, V <sub>IL</sub>			0.8			0.8	V
High Level Output Voltage, VOH			5.5			5.5	V
Low Level Output Current, IOL	Langue much		12	o pop iligo		24	m/

#### Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Тур	Max	Unit
VIK	Input Clamp Voltage	$V_{CC} = 4.5V, I_{I} = -18mA$				-1.5	V
ЮН	High Level Output Current	$V_{CC} = 4.5V, V_{OH}$	H = 5.5V			100	μΑ
VOL	Low Level Output Voltage	$V_{CC} = 4.5V$	54/74ALS I <sub>OL</sub> = 12mA		0.25	0.4	٧
	of or other	Blateau Blateau	74 ALS I <sub>OL</sub> = 24mA		0.35	0.5	V
l <sub>l</sub>	Max High Input Current	$V_{CC} = 5.5V, V_{IH}$	= 7V			0.1	mA
Ιн	High Level Input Current	$V_{CC} = 5.5V, V_{IH}$	= 2.7V			20	μΑ
ŊĽ	Low Level Input Current	$V_{CC} = 5.5V, V_{IL}$	$V_{CC} = 5.5V, V_{ L} = 0.4V$			-0.2	mA
ICC	Supply Current	V <sub>CC</sub> = 5.5V	Outputs High	nal Jastillad	0.53	off weight	mA
			Outputs Low		1.3		mA

# Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter		DI	M54ALS10	35	DM74ALS1035			
	Conditions	Min	Тур	Max	Min	Тур	Max	Unit
TPLH, Propagation delay time. Low to high Level Output	$V_{CC} = 4.5 \text{ to } 5.5V$ $R_L = 667 \Omega$ , $C_L = 50 \text{ pF}$ .	7	12	30	7	12	25	ns
TPHL, Propagation delay time. High to low Level Output	1	2	4.5	12	2	4.5	9	ns

National Semiconductor

**Preliminary** 

# DM54ALS/DM74ALS1240, 1241, 1242, 1243, 1244 TRI-STATE® Bus Drivers/Receivers

#### **General Description**

This family of Advance Low Power Schottky TRI-STATE Bus circuits are designed to provide either bidirectional or unidirectional buffer interface in Memory, Microprocessor, and Communication Systems. The output characteristics of the circuits have low impedance sufficient to drive terminated transmission lines. The input characteristics of the circuits likewise have a high impedance so it will not significantly load the transmission line. The package contains eight TRI-STATE buffers organized with four buffers having a common TRI-STATE enable gate. The ALS1240, 1241 and 1244 are eight wide in a 20 pin package, and may be used as a 4 wide bidirectional or eight wide unidirectional. The ALS1242 and 1243 are organized four wide bidirectional in a 14 pin package. The buffer selection includes inverting and non-inverting, with enable or disable TRI-STATE control. The TRI-STATE circuitry contains a feature that maintains the buffers in TRI-STATE until the power supply (VCC) is greater than 3V. This feature prevents the buffers from glitching the system bus during power up or

- Improved Switching Performance with Less Power Dissipation Compared with 54/74LS Counterpart.
- Functional and Pin Compatible with 54/74LS Counterpart.
- Switching Response Specified Into 500 ohm and 50 pF.
- Low Level Drive Current 74ALS-1 24ma, 74ALS 16ma, 54ALS 8ma
- Glitch Free Bus During Power Up/Down.
- Specified To Interface With CMOS At VOH = V<sub>CC</sub> - 2V.

#### **Absolute Maximum Ratings**

 Supply Voltage, VCC
 7.0V

 Input Voltage
 7.0V

 Operating Free Air Temperature Range
 DM54ALS
 -55°C to 125°C

 DM74ALS
 0°C to 70.C

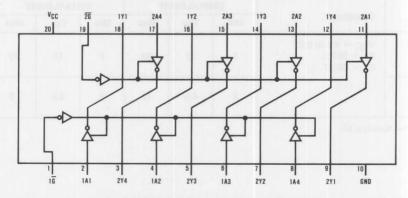
 Storage Temperature Range
 -65°C to +150°C

 Lead Temperature
 (Soldering, 10 seconds)
 +300°C

#### **Features**

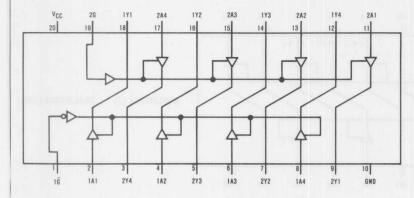
- Lower Power Version of 54ALS240/241/242/243/244
- Advanced Low Power Oxide-Isolated, Ion-Implanted Schottky TTL Process.

#### **Connection Diagram**

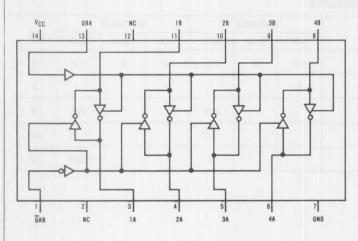


54ALS1240 (J) 74ALS1240 (J,N)

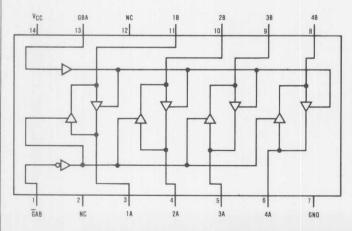
#### **Connection Diagrams**



54ALS1241 (J) 74ALS1241 (J,N)

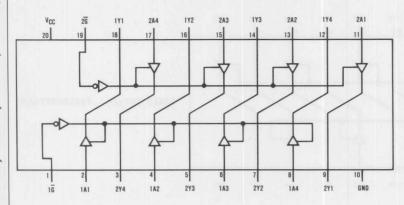


54ALS1242 (J) 74ALS1242 (J,N



54ALS1243 (J) 74ALS1243 (J,N)

# **Connection Diagrams**



54ALS1244 (J) 74ALS1244 (J,N)

# **Recommended Operating Conditions**

		DM54ALS					
Parameter	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage, VCC	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, VIH	2			2			V
Low Level Input Voltage, V <sub>IL</sub>			0.8			0.8	V
High Level Output Current, IOH			-12			-15	mA
Low Level Output Current, IOL			8			16/24*	mA

<sup>\*</sup> Applies to 74ALS-1 options.

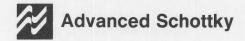
	Parameter	Conditions	Min	Тур	Max	Uni
VIK	Input Clamp Voltage	$V_{CC} = 4.5V, I_{IN} = -18mA$		deside (i	-1.5	٧
VOH	High Level Output Voltage	$V_{CC} = 4.5V, I_{OH} = -3mA$ $V_{CC} = 4.5V, I_{OH} = -15mA$ $I_{OH} = -400\mu A$	2.4 2.0 V <sub>CC</sub> -2	3.2 2.3	Hank we Toron D School-steel	V V V
VOL	Low Level Output Voltage	V <sub>CC</sub> = 4.5V I <sub>OL</sub> = 8mA 54/74 I <sub>OL</sub> = 16mA 74 I <sub>OL</sub> = 24mA 74-1		.25 .35 .35	.40 .50 .50	V V V
liX	Input Current at Max Input Voltage	$V_{CC} = 5.5V, V_{IN} = 7V$			100	μΑ
IIH	High Level Input Current	$V_{CC} = 5.5V, V_{IN} = 2.7V$			20	μΑ
IIL	Low Level Input Current	$V_{CC} = 5.5V, V_{IN} = 0.4V$		p) dist	-200	μΑ
lozh	High Level TRI-STATE® Output Current	$V_{CC} = 5.5V, V = 2.7V$			20	μΑ
lozL	Low Level TRI-STATE Output Current	V <sub>CC</sub> = 5.5V, V = .4V			-20	μΑ
IOD	Output Drive Current	$V_{CC} = 5.5V, V_{OUT} = 2.25V$	-30		-110	m/
Icc	Supply Current	V <sub>CC</sub> = 5.5V 54/74ALS1240 Outputs High Outputs Low TRI-STATE			Iden.	m.A
Icc	Supply Current	V <sub>CC</sub> = 5.5V 54/74ALS1241 Outputs High Outputs Low TRI-STATE			off hopes diss of both	m.A
lcc	Supply Current	V <sub>CC</sub> = 5.5V 54/74ALS1242 A Port Outputs High A Port Outputs Low TRI-STATE	en eun en eur		ing hughest land hughest land land	m.
lcc	Supply Current	V <sub>CC</sub> = 5.5V 54/74ALS1243 A Port Outputs High A Port Outputs Low TRI-STATE		0.1 600	oši togod	m.
ICC	Supply Current	V <sub>CC</sub> = 5.5V 54/74ALS1244 Outputs High Outputs Low TRI-STATE	i ka		HU Ample Hue. HIS Hop. C	m.

#### Switching Characteristics over recommended operating free air temperature range (Notes 1, 2)

Parameter	Circuit		74ALS			54ALS		
(Propagation Delay Time)	Configuration	Min	Тур	Max	Min	Тур	Max	Unit
Г <sub>РLН</sub> , Low-to-High Level Output Г <sub>РНL</sub> , High-to-Low				50 Y				ns
Level Output	ALS 1240, 1242							ns
T <sub>PLH</sub> , Low-to-High Level Output T <sub>PHL</sub> , High-to-Low								ns
Level Output	ALS 1241, 1243, 1244	· Way	V VBE	tor j				ns
T <sub>PZL</sub> , Output Enable to Low Level		WILL	N NA S					ns
TPZH, Output Enable to High Level		V80	NEE.	eqr.	(Aumu)	uniter i		ns
TpLZ, Output Disable From Low Level	>o	4.4-	v mil-	100	OSTARE-			ns
TPHZ, Output Disable From High Level	ALS 1240, 1242	. Mil	v ve di	Last I	- STATE	ATION		ns
T <sub>PZL</sub> , Output Enable to Low Level						MATERIAL I		ns
TPZH, Output Enable to High Level		19 T 19	A VER	108Y				ns
T <sub>PLZ</sub> , Output Disable From Low Level			1000	08				ns
T <sub>PHZ</sub> , Output Disable From High Level	ALS 1242		3111					ns
TpzL, Output Enable to		LASTPA	- 5/3/8 2-1/9/	t conf				ns
TPZH, Output Enable to High Level			HIM	GART.				ns
T <sub>PLZ</sub> , Output Disable From Low Level		Like The	V8.6	291		F10,0		ns
TPHZ, Output Disable From High Level	ALS 1241, 1243, 1244		C LOUIS OF STREET	169 A B-10 F y				ns
TpzL, Output Enable to		Theorem	16.6	13971				115
Low Level TPZH, Output Enable to	<b>→</b>	1	S que					ns
High Level T <sub>PLZ</sub> , Output Disable From		- station to see	lyan .					ns
Low Level TPHZ, Output Disable From			Control of					ns
High Level	ALS 1241, 1242							ns

NOTE 1: See notes pg. 1-iii, figures pg. 3-2.

NOTE 2: Switching characteristic conditions are  $V_{CC}=4.5V$  to 5.5V,  $R_L=500\Omega$ ,  $C_L=50pF$ .



The DM54/74AS family of devices are designed to meet the needs of system designers who require the ultimate in speed. AS achieves the fastest prop delays bipolar technology can offer (2 ns per gate). The AS family also offers significant reduction in power dissipation (8 mw per gate) over present Schottky (54/74S) with toggle rate capability of up to 200 MHz.

The AS family is TTL pinout compatible and offers Schottky (54/74S) drive capability with better fan out, higher noise immunity and faster operation.

For maximum design flexibility and elimination of special drawings, the AS family will be introduced with  $\pm$  10% VCC over the military and commercial full temp range as standard product. Furthermore, all switching characteristics are guaranteed over the full temperature and VCC range.



The Transfer of AAC is all the devices are designed to meet the search of eyerem congreges who require the transfer is speed.

AS are levies the task of proof design become retricted in speed.

Of the property of parent of any parent standard present Scholide in AAC and present Scholide (SAA).

The AS benely by Till, places compatible and often Bolotting GMZ4. Suchive engan lidyounds better han out, buying noise annu-

Figure skijment niestę stanklijtiky end othernation of Apatolei ritere inge, I ne Apapelly se the entrodyced own a 1075 Vgc svenske multar mend commercial full semp mage as standard product. Figure singue, all eigh coing dramaters and guern stand-avar the file tum company and Victo as our se



# **ADVANCED SCHOTTKY**

## **Absolute Maximum Ratings (Note 1)**

 Supply Voltage, V<sub>CC</sub> (1)
 7V

 Input Voltage, V<sub>I</sub>: All Inputs
 7V

 I/O Ports
 5.5V

Off State (High Level) Voltage Applied

to Open-Collector Outputs 7V High Level Voltage Applied to 3-State Outputs 5.5V

Operating Free-Air Temperature Range:

SN54AS -55°C to 125°C SN74AS 0°C to 70°C

Storage Temperature Range -65°C to 150°C

## **Recommended Operating Conditions**

		Star	ndard Ou	itput	Bu	ffer Out	out	Bus			
Parameter		Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Unit
Supply Voltage	54/74AS	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	٧
High Level Input Voltage, VIH	54/74AS	2.0			2.0			2.0			V
Low Level Input Voltage, V <sub>IL</sub>	54/74AS			0.8			0.8			0.8	٧
High Level Output	54AS			-2.0			-12			-40	mA
Voltage, IOH (2)	74AS			-2.0			-15			-48	mA
High Level Output Current, VOH (3)	54/74AS			5.5			5.5			5.5	٧
Low Level Output	54AS			20			32			40	mA
Current, IOL	74AS			20			48			48	mA
Operating Free-Air	54AS	-55		125	-55		125	-55	Ha	125	°C
Temperature, TA	74AS	0		70	0		70	0		70	°C

**ADVANCED SCHOTTKY** 

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

			Standard Output Buffer Ou		ffer Outp	ut	Bus	us Driver Output					
	Parameter	Conditions		Min	Typ(4)	Max	Min	Typ(4)	Max	Min	Typ(4)	Max	Unit
VIK	Input Clamp Voltage	$V_{CC} = 4.5V$ $I_{I} = -18\text{mA}$				-1.2			-1.2			-1.2	V
VOH	High Level Output Voltage (2)	$I_{OH} = MAX$ $V_{CC} = 4.5V$					2.4	3.2		2			V
		$I_{OH} = -2.0m$	ıA .	V <sub>CC</sub> -2V			V <sub>CC</sub> -2V			V <sub>CC</sub> -2V			V
ЮН	High Level Output Current (3)	$V_{CC} = 4.5V  V_{OH} = 5.5V$				0.1			0.1			0.1	mA
VOL	Low Level Output Voltage	$V_{CC} = 4.5V$ $I_{OL} = MAX$			0.35	0.5		0.35	0.5		0.35	0.5	V
l <sub>l</sub>	Input Current at Maximum Input Voltage	$V_{CC} = 5.5V$ $V_{I} = 7V$				0.1			0.1			0.1	mA
ΊΗ	High Level Input Current	$V_{CC} = 5.5V$ $V_{I} = 2.7V$				20			20			20	μΑ
ЦС	Low Level Input Current	$V_{CC} = 5.5V$ $V_{IL} = 0.5V$				-1.0			-1.0			-1.0	mA
10	Output Current (5)	$V_{CC} = 5.5V$ $V_{O} = 2.25V$		-30		-110	-30		-110	-30		-110	mA
lozh	Off-State Output Current, High Level Voltage Applied (6)	$V_{CC} = 5.5V$ $V_{O} = 2.7V$				3 4			50			50	μΑ
lozL	Off-State Output Current,	V <sub>CC</sub> = 5.5V	I/O Ports			A IA			-1.0			-1.0	mA
	Low Level Voltage Applied (6)	$V_O = 0.5V$	Non-I/O						-50		138	-50	μΑ
Icc	Supply Current (7)	$V_{CC} = 5.5V$											mA

NOTE 1: Voltage values are with respect to network ground terminal.

NOTE 2: Does not apply to open-collector outputs.

NOTE 3: Applies only to open-collector outputs.

NOTE 4: All typical numbers are at  $V_{CC} = 5V$ ,  $T_A = 25$ °C.

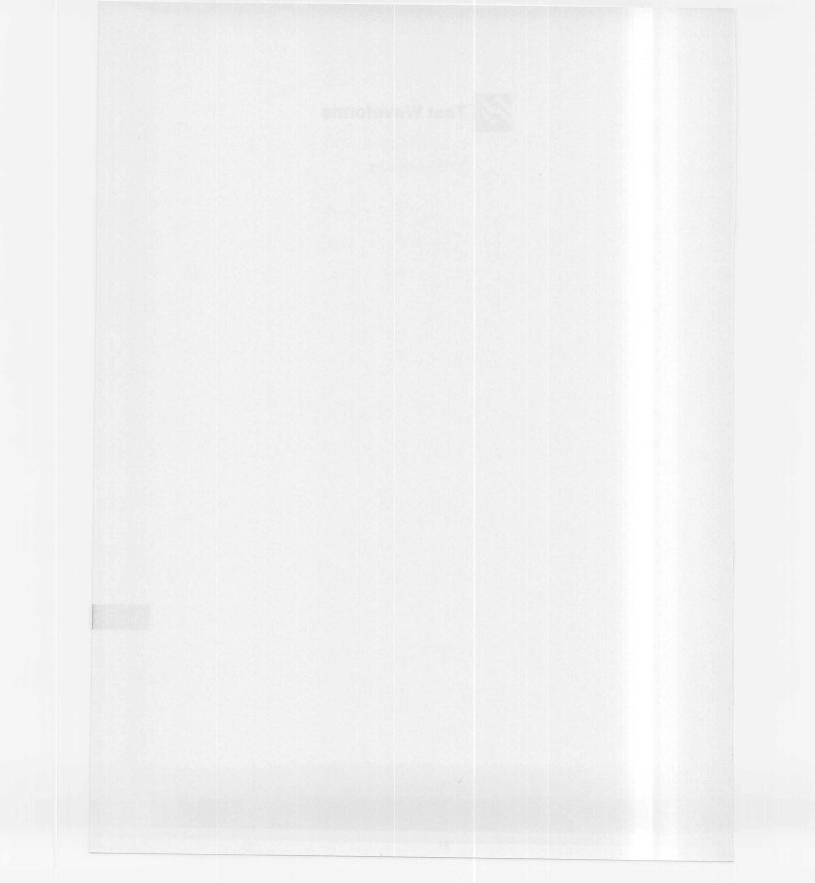
NOTE 5: The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current, IOS.

NOTE 6: Applies only to TRI-STATE outputs.

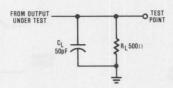
NOTE 7: Refer to individual data sheet for I<sub>CC</sub> limits.



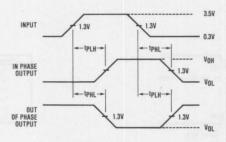
3



54ALS00, 02, 04, 08, 10, 11, 20, 21, 27, 28, 30, 32, 37, 40, 133, 138, 151, 153, 157, 158, 352, 520, 521, 804, 805, 808, 832, 1000, 1002, 1004, 1008, 1010, 1011, 1020, 1032, 1034



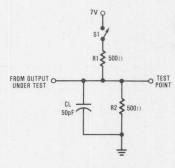
LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS



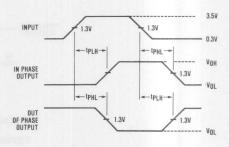
VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES

J

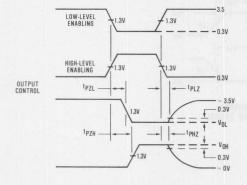
54ALS240, 241, 242, 243, 244, 251, 253, 257, 258, 353, 640, 641, 642, 643, 644, 645, 1240, 1241, 1242, 1243, 1244



LOAD CIRCUIT FOR TRI-STATE OUTPUTS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES

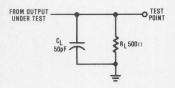


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, TRI-STATE OUTPUTS

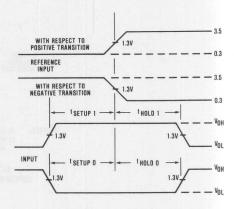
Parameter	S1 Switch Position	
T <sub>PLH</sub>	OPEN	
T <sub>PHL</sub>	OPEN	
TPHZ	OPEN	
T <sub>PZH</sub>	OPEN	
T <sub>PLZ</sub>	CLOSED	
TPZL	CLOSED	

NOTE: All input pulses are supplied by generators having the following characteristics: frequency = 1MHz,  $Z_{OUT} = 50~\Omega$ ,  $t_f = t_f = 2$ ns.

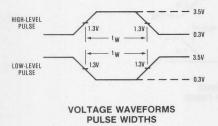
54ALS74, 109, 112, 113, 114, 131, 137, 160, 161, 162, 163, 168, 169, 174, 175, 273

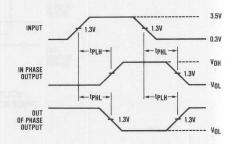


LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES

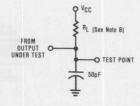




VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES

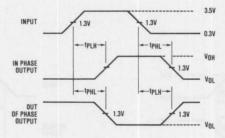
3

NOTE: All input pulses are supplied by generators having the following characteristics: frequency = 1MHz,  $Z_{OUT} = 50 \Omega$ ,  $t_f = t_f = 2 ns$ .



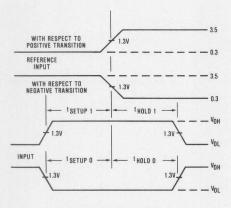
 $\begin{array}{ll} \text{NOTES:} & \text{A. C}_L \text{ includes probe and jig capacitance} \\ \text{B. R}_L = 2 \text{K} \Omega \text{ for standard outputs} \\ & \text{R}_L = 667 \Omega \text{ for buffered outputs} \end{array}$ 

# LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUTS

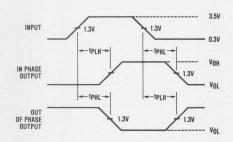


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTE: All input pulses are supplied by generators having the following characteristics: frequency = 1 MHz,  $Z_{OUT} = 50~\Omega$ ,  $t_T = t_f = 2 \text{ns}$ .

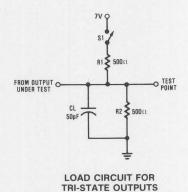


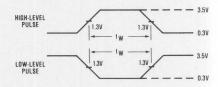
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



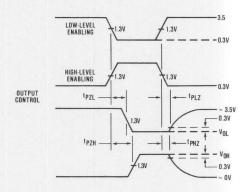
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

Parameter	S1 Switch Position
TPLH	OPEN
TPHL	OPEN
TPHZ	OPEN
TPZH	OPEN
TPLZ	CLOSED
TPZL	CLOSED



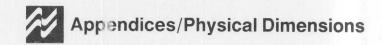


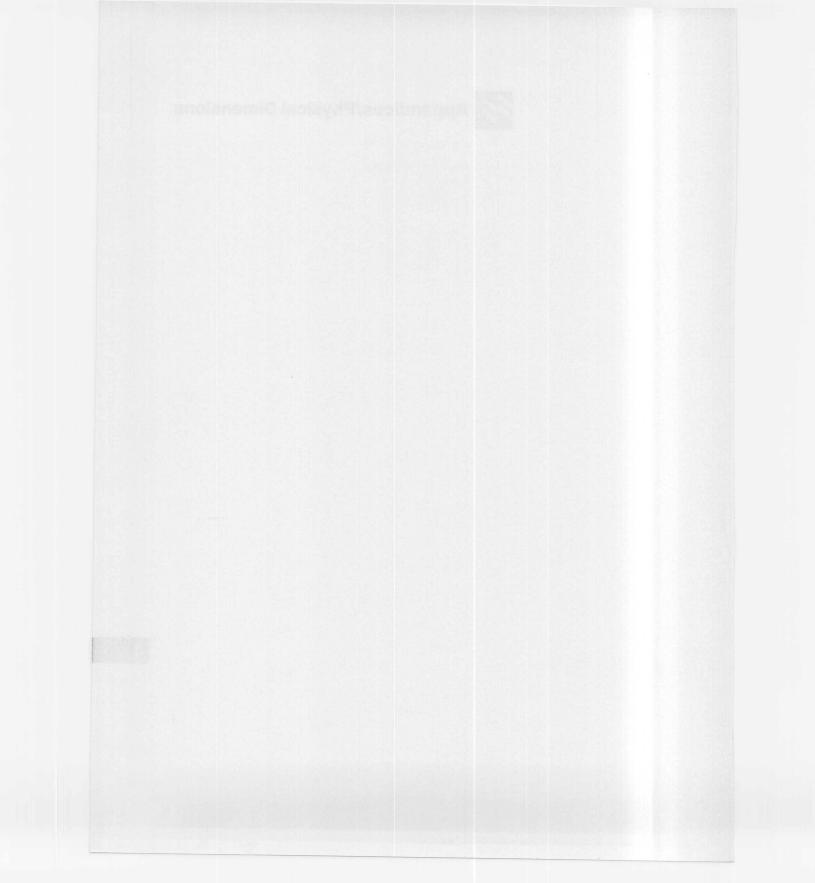
VOLTAGE WAVEFORMS PULSE WIDTHS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, TRI-STATE OUTPUTS

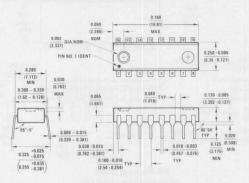
**NOTE:** All input pulses are supplied by generators having the following characteristics: frequency = 1MHz,  $Z_{OUT} = 50 \Omega$ ,  $t_r = t_f = 2$ ns.



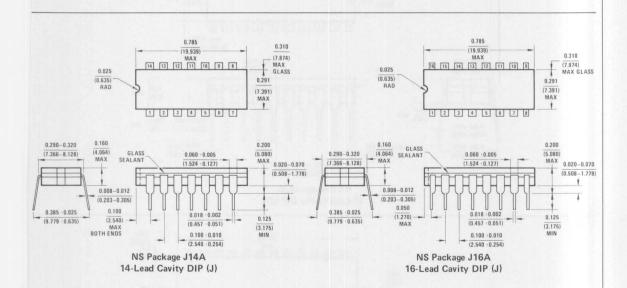


### **Physical Dimensions**

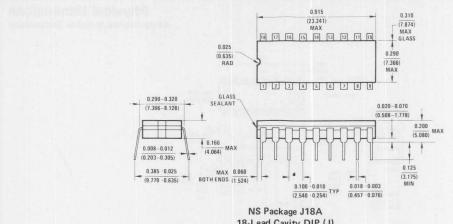
All dimensions in inches (millimeters)



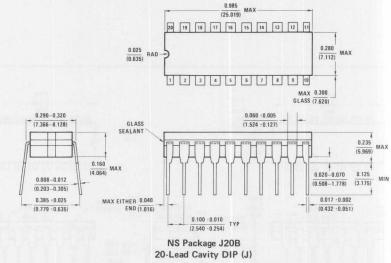
NS Package N16E 16-Lead Molded DIP (N)

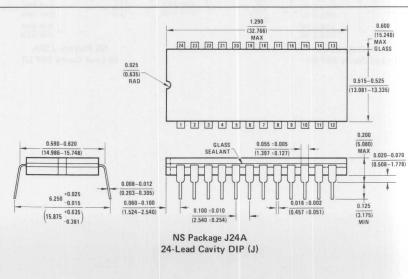


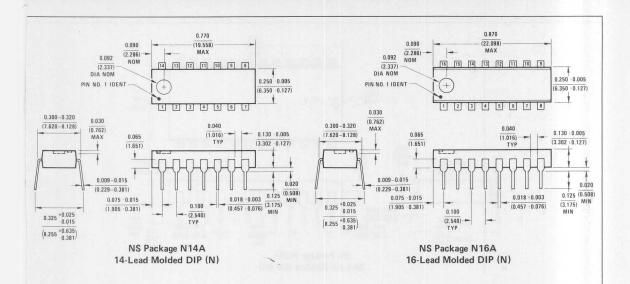
4

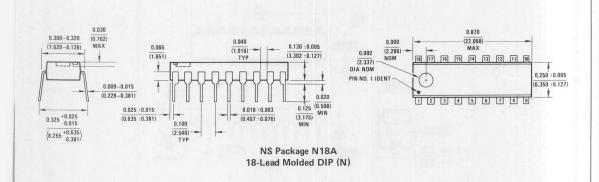


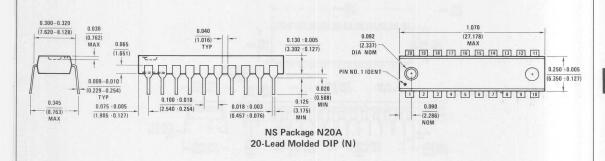
18-Lead Cavity DIP (J)



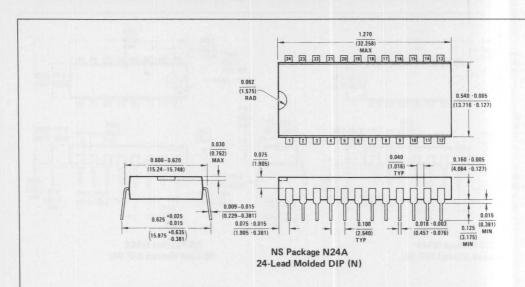


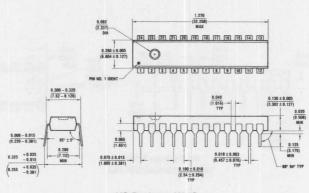




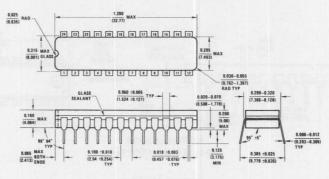


4





NS Package N24C 24-Lead Molded DIP (N)



NS Package J24F 24-Lead CERDIP (J)